

**Inter-processor Communication module**

**Design spec**

**(Rev. 1.0)**

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**Revision History**

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| --- | --- | --- | --- | --- |
| **Rev.** | **Release Date** | **DCC No.** | **Author** | **Change** |
| 0.1 | 2016-04-25 |  | Roland Lou | Initial Release |
| 0.2 | 2016-06-16 |  | Yu Yang | 5.3.9, 5.3.10 in v0.1 modified  5.1 Register memory mapping new  6. Interface new  Interrupt to ARM changed to 8 bits |
| 0.3 | 2016-06-21 |  | Yu Yang | Share RAM size changed to 32Kbyte.  Page size changed to 1KByte |
| 0.4 | 2016-07-25 |  | Yu Yang | \*IPCRESP changed to \*IPCDATA1.  \*IPCDATA changed to \*IPCDATA0 |
| 1.0 | 2017-05-10 |  | Yu Yang | make IPCTMRSCALER & IPCTMRCONT readable to A7 & PLC core  Each core can set its own IPC INT flag for debugging purpose  Additional INT output which is triggered when receiving ACK from communicating core |
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# General Description

The Inter Processor Communications (IPC) module facilitates communication between the ARM and DSPs subsystems. This section details the IPC mechanisms that the ARM subsystem and DSPs subsystem can use to request/share information between the subsystems and notify the status of any dependent tasks between the subsystems.

This module consists of four main features:

* IPC flags and interrupts
* Shared RAM
* IPC Message registers
* Free running timer

# Interface Description

The processors use their respective AHB buses to access the CSR registers for control and message transfer and the shared RAM for data transfer. In addition, interrupts for inter-processor communication are also provided.



Figure 1 IPC interface diagram

# Functional Description



### IPC flags and interrupts

For all the CPU cores, there are 16 IPC handshake channels from one core to the other core and vice versa to enable communication between the cores based on software flags. Out of these 16, eight channels (0 through 7) can be enabled to generate IPC interrupts to the other core. These handshake channels can be used along with the shared RAM to build a software handshake mechanism between the cores.

Figure below shows the IPC flag messaging and interrupt mechanism. (Here the communication between ARM and RF\_DSP taken as an example)



Figure 2 Messaging with IPC Flags and Interrupts

The A7TORF IPC is used by the ARM Subsystem to send events to the RF DSP Subsystem. The A7TORF IPC typically sends events to the RF DSP Subsystem by using the following registers: A7TORFIPCSET, A7TORFIPCFLG/A7TORFIPCSTS, and A7TORFIPCACK/A7TORFIPCCLR. Each of the 16 bits of these registers represents 16 independent channels through which the Cortex-A7 CPU can send up to 16 events to the RF DSP via software handshaking. Additionally, the first 8 bits of the A7TORF IPC registers are supplemented with interrupts.

To send an event via channel 2 from Cortex-A7 to RF DSP, for example, the Cortex-A7 and RF DSP CPUs use bit 2 of the A7TORFIPCSET, A7TORFIPCFLG/A7TORFIPCSTS, and A7TORFIPCACK/A7TORFIPCCLR registers. The handshake starts with the Cortex-A7 polling bit 2 of the A7TORFIPCFLG register to make sure bit 2 is ‘0’. Next, the Cortex-A7 writes a ‘1’ into bit 2 of the A7TORFIPCSET register to start the handshake. In the mean time, the DF DSP is continually polling the A7TORFIPCSTS register while waiting for the message. As soon as the Cortex-A7 writes ‘1’ to bit 2 of the A7TORFIPCSET register, bit 2 of A7TORFIPCFLG/A7TORFIPCSTS also turns ‘1’, thus announcing the event to the RF DSP. As soon as the RF DSP CPU reads a ‘1’ from the A7TORFIPCSTS register, the RF DSP CPU should acknowledge by writing a ‘1’ to bit 2 of the A7TORFIPCACK register, which in turn, clears bit 2 of the A7TORFIPCFLG/A7TORFIPCSTS register, enabling the Cortex-A7 to send another message. Since the first eight channels (bits <7:0>) are backed up by interrupts, both processors in the above example can use IPC interrupt 2 instead of polling to increase performance.

As for the A7TORFIPCCLR register, Cortex-A7 can set bits in the A7TORFIPCCLR register to clear corresponding flags (flag bit in A7TORFIPCFLG and status bit in A7TORFIPCSTS) that the A7 has set previously using the A7TORFIPCSET register. Generally, the RF DSP should acknowledge the A7TORFIPC request using the A7TORFIPCACK register which will clear the A7TORFIPCFLG bits and A7TORFIPCSTS bits. However, at times when the A7 did not receive any acknowledgement from the RF DSP about the reception of a message in an expected duration, the A7 application software might want to clear the A7TORFIPC flag request that it set earlier. In such a scenario, the A7 can clear the flag requests that are raised previously by setting corresponding bits in the A7TORFIPCCLR register.

Note that the A7TORFIPCSET registers are write-only by the A7 and will always read back as 0. The A7 should read the A7TORFIPCFLG register to see pending requests. The A7TORFIPCFLG and A7TORFIPCSTS registers are read-only and will always reflect the current status of the corresponding IPC flag whether it has been requested or cleared. The A7TORFIPCCLR and A7TORFIPCACK bits are write-only and will always read back as 0.

A similar handshake is also used when sending data (not just event) from the ARM Subsystem to the RF DSP Subsystem, but with two additional steps. Before setting a bit in the A7TORFIPCSET register, the Cortex-A7 should first load the A7TORF shared RAM with a block of data that is to be made available to the RF DSP. In the second additional step, the RF DSP should read the data before setting a bit in the A7TORFIPCACK register. This way, no data gets lost during multiple data transfers through a given block of the shared RAM.

The RFTOA7 IPC is used by the RF DSP Subsystem to send events to the ARM Subsystem. The RFTOA7 IPC typically sends events to the ARM Subsystem by using the following three registers: RFTOA7IPCSET, RFTOA7IPCFLG/ RFTOA7IPCSTS, and RFTOA7IPCACK/RFTOA7IPCCLR. The process is exactly the same as that for the A7TORF IPC communication above.

Same as the mechanism above, the following registers are used for the IPC communications between A7 and PLC DSP, and DSP cores:

A7TOPLCIPCSET, A7TOPLCIPCCLR, A7TOPLCIPCFLG, A7TOPLCIPCSTS, A7TOPLCIPCACK;

PLCTOA7IPCSET, PLCTOA7IPCCLR, PLCTOA7IPCFLG, PLCTOA7IPCSTS, PLCTOA7IPCACK;

RFTOPLCIPCSET, RFTOPLCIPCCLR, RFTOPLCIPCFLG, RFTOPLCIPCSTS, RFTOPLCIPCACK;

PLCTORFIPCSET, PLCTORFIPCCLR, PLCTORFIPCFLG, PLCTORFIPCSTS, PLCTORFIPCACK;

### Shared RAM

32k Bytes shared memory between Host ARM, RF DSP and PLC DSP is available in the device. And the 32K RAM can be partitioned into 32 1K bytes pages. Each page can be owned by the ARM core, RF DSP or PLC DSP based on the configuration of respective bits (two bits for each memory page) in the SRMSEL1&0 register. When a page is owned by the A7 subsystem, the A7 CPU and its DMA have full access to that RAM block, whereas the DSP CPUs and DMAs have only read access to that RAM page (no write access).

Since all the cores can get the ownership of any shared memory page, the following semaphore mechanism is used to allocate the shared memory pages in case of conflicts.



Figure 3 Shared RAM semaphore mechanism

The 32 memory pages semaphore state can be read by all the cores through status register SRMSEL1&0 (2 bits per page). If any core wants to get the ownership of some page, it will firstly check the status register SRMSEL1/0. If the memory page is free (semaphore state = “00”), then the core should write the SRPxxREQ register with respective value to get the ownership. Again the status register SRMSEL1/0 should be read to check if the page’s ownership obtained or not in case two or more cores request the page simultaneously. The priority for the simultaneous memory ownership request is A7 firstly served, then RF DSP, and PLC DSP lastly.

After the core gets the memory pages ownership, the software designers have the freedom to decide the usage of the RAM: buffer for data movement between cores or key variables publishing space to other cores.

### IPC message registers

IPC message registers provide a simple and flexible way to send messages between the CPU cores. There are four dedicated IPC message registers for each core-to-core communication. There is not any specific hardware definition for the usage of these registers. The user's application software has to define the usage of these registers. These registers can be used like mailboxes to send short messages back and forth between cores when the software cannot use memories for inter processor communication. Or they can be used to pass frame information such as start address, number of words, message type codes etc for long messages written to the shared RAM. IPC Message registers on each of the subsystems are accessible by other subsystems.

IPC Message registers that are used to convey messages between the cores are given as:

A7TORFIPCCOMM, A7TORFIPCADDR, A7TORFIPCDATA0, A7TORFIPCDATA1.

A7TOPLCIPCCOMM, A7TOPLCIPCADDR, A7TOPLCIPCDATA0, A7TOPLCIPC DATA1.

RFTOA7IPCCOMM, RFTOA7IPCADDR, RFTOA7IPCDATA0, RFTOA7IPC DATA1.

RFTOPLCIPCCOMM, RFTOPLCIPCADDR, RFTOPLCIPCDATA0, RFTOPLCIPC DATA1.

PLCTOA7IPCCOMM, PLCTOA7IPCADDR, PLCTOA7IPCDATA0, PLCTOA7IPC DATA1.

PLCTORFIPCCOMM, PLCTORFIPCADDR, PLCTORFIPCDATA0, PLCTORFIPC DATA1.

### Free run timer

A 64-bit free running timer is present in the device and can be used to timestamp IPC events between processors. This 64-bit IPCCOUNTERL(32-bit)/ IPCCOUNTERH(32-bit) is clocked by the shared resources clock and is readable by the A7 and the DSPs on their respective memory maps. These counter registers are reset to zero on reset.

Because the counter is 64-bits and the A7/DSPs can only read 32-bits at a time, an issue can arise when reading the counters separately. If the low 32-bit counter is read just before it overflows and then the high 32-bit counter is read, the combined values read will be incorrect. To solve this, a snapshot for the high 32-bits counter is taken when a read is performed on the IPCCOUNTERL register. When the A7/DSPs read the IPCOUNTERH, the snapshot is fed back to the user instead of the current value in the IPCOUNTERH register. Therefore, the user application software must always read IPCCOUNTERL first and then read IPCCOUNTERH.

Besides, the following features are also supported:

* Programmable prescalers from main CPU clock
* 1us resolution 64 bit timer
* Be configurable as count up or count down.

# Examples for software IPC procedures

The below are given suggested examples of the sequence to be followed in software for IPC.



### IPC with interrupts

Below is an example procedure for IPC usage when the A7 CPU wants to get some information from the RF DSP using A7TORFIPCINT0:

* The A7 writes a ‘1’ in bit 0 of the A7TORFIPCSET register and this generates the A7TORFIPCINT0 to the RF DSP through the PVIC.
* Bit 0 in the A7TORFIPCFLG and A7TORFIPCSTS registers get set. The RF DSP services the interrupt and in the corresponding ISR, the RF DSP loads the pre-defined information in the shared RAM (user application has to define the ISR functionality).
* The RF DSP clears this A7TORFIPC request by writing a ‘1’ to bit 0 of the A7TORFIPCACK register at the end of the ISR.
* The A7 polls the status of bit 0 in the A7TORFIPCFLG register and until the status is ‘1’, it understands that the RF DSP has not serviced the interrupt. When the status becomes ‘0’, it understands that the RF DSP has serviced the interrupt and reads the RAM from the predefined location and gathers the requested information

### IPC with flags

Below is an example procedure for IPC usage when the RF DSP wants to communicate a message to the A7 about a shared resource using RFTOA7IPC-flag 9:

* The RF DSP writes a ‘1’ to bit 9 of the RFTOA7IPCSET register to indicate that the A7 can go ahead and use a particular resource as the RF DSP is done with using that resource. (In user application software, IPC flag 9 will be tied to a particular resource and task.)
* When the A7 wants to use this resource, it will read bit 9 of the RFTOA7IPCSTS register. When the A7 reads bit 9 of the RFTOA7IPCSTS register as a ‘1’, it uses shared resource tied to IPC flag 9 in the predefined manner.
* After completing the task using the shared resource tied with IPC9, the A7 CPU will clear the flag by writing ‘1’ to bit 9 of RFTOA7IPCACK.
* When bit 9 of the RFTOA7IPCFLG register is a ‘1’ and the flag is not yet cleared by the A7 CPU, if the RF DSP reads bit 9 of the RFTOA7IPCFLG register, the RF DSP reads it as a ‘1’. When the flag has been cleared by the A7, bit 9 of the RFTOA7IPCFLG will read ‘0’. Based on this, RF DSP software proceeds accordingly for its task.

# Register Description



### Register memory mapping

### A7IPC Register memory mapping

|  |  |
| --- | --- |
| AHB Master | AHB Base address |
| A7 AHB | 0xC230\_0000 |

|  |  |  |
| --- | --- | --- |
| Register Name | Offset | Description |
| A7TORFIPCCOMM | 12’h000 | A7 core to RFDSP core IPC command register |
| A7TORFIPCADDR | 12’h004 | A7 core to RFDSP core IPC address register |
| A7TORFIPCDATA0 | 12’h008 | A7 core to RFDSP core IPC data0 register |
| A7TORFIPCDATA1 | 12’h00c | A7 core to RFDSP core IPC data1 register |
| A7TOPLCIPCCOMM | 12’h010 | A7 core to PLCDSP core IPC command register |
| A7TOPLCIPCADDR | 12’h014 | A7 core to PLCDSP core IPC address register |
| A7TOPLCIPCDATA0 | 12’h018 | A7 core to PLCDSP core IPC data0 register |
| A7TOPLCIPCDATA1 | 12’h01c | A7 core to PLCDSP core IPC data1 register |
| RFTOA7IPCCOMM | 12’h020 | RFDSP core to A7 core IPC command register |
| RFTOA7IPCADDR | 12’h024 | RFDSP core to A7 core IPC address register |
| RFTOA7IPCDATA0 | 12’h028 | RFDSP core to A7 core IPC data0 register |
| RFTOA7IPCDATA1 | 12’h02c | RFDSP core to A7 core IPC data1 register |
| Reserved | 12’h030~  12’h3c |  |
| PLCTOA7IPCCOMM | 12’h040 | PLCDSP core to A7 core IPC command register |
| PLCTOA7IPCADDR | 12’h044 | PLCDSP core to A7 core IPC address register |
| PLCTOA7IPCDATA0 | 12’h048 | PLCDSP core to A7 core IPC data0 register |
| PLCTOA7IPCDATA1 | 12’h04c | PLCDSP core to A7 core IPC data1 register |
| Reserved | 12’h050~  12’h7c |  |
| IPCTMRSCALER | 12’h080 | Free running 64bit timestamp counter prescaler register. |
| IPCCOUNTERL | 12’h084 | Free running 64bit timestamp counter low register. |
| IPCCOUNTERH | 12’h088 | Free running 64bit timestamp counter high register. |
| IPCTMRCONT | 12’h08c | Free running 64bit timestamp control register. |
| SRMSEL0 | 12’h090 | Shared RAM pages’ ownership (master selection) status register0 |
| SRMSEL1 | 12’h094 | Shared RAM pages’ ownership (master selection) status register1 |
| Reserved | 12’h098~  12’h0fc |  |
| A7TORFIPCSET | 12’h100 | A7 core to RFDSP core IPC set register |
| A7TORFIPCCLR | 12’h104 | A7 core to RFDSP core IPC clear register |
| A7TORFIPCFLG | 12’h108 | A7 core to RFDSP core IPC flags register |
| RFTOA7IPCACK | 12’h10c | RFDSP core to A7 core IPC event acknowledge register. |
| RFTOA7IPCSTS | 12’h110 | RFDSP core to A7 core IPC event status register. |
| A7TOPLCIPCSET | 12’h114 | A7 core to PLCDSP core IPC set register |
| A7TOPLCIPCCLR | 12’h118 | A7 core to PLCDSP core IPC clear register |
| A7TOPLCIPCFLG | 12’h11c | A7 core to PLCDSP core IPC flags register |
| PLCTOA7IPCACK | 12’h120 | PLCDSP core to A7 core IPC event acknowledge register. |
| PLCTOA7IPCSTS | 12’h124 | PLCDSP core to A7 core IPC event status register |
| Reserved | 12’h128~  12’h12c |  |
| RFTOA7IPCTEST | 12’h130 | RFDSP core to A7 core IPC set register for testing |
| PLCTOA7IPCTEST | 12’h134 | PLCDSP core to A7 core IPC set register for testing |
| Reserved | 12’h138~  12’h13c |  |
| RFTOA7ACK\_INT\_CLR | 12’h140 | RFDSP core to A7 core ACK interrupt clear |
| PLCTOA7ACK\_INT\_CLR | 12’h144 | PLCDSP core to A7 core ACK interrupt clear |
| Reserved | 12’h148~  12’h1fc |  |
| A7SRP00REQ | 12’h200 | Shared RAM page00 ownership request semaphore register |
| A7SRP01REQ | 12’h204 | Shared RAM page01 ownership request semaphore register |
| A7SRP02REQ | 12’h208 | Shared RAM page02 ownership request semaphore register |
| A7SRP03REQ | 12’h20c | Shared RAM page03 ownership request semaphore register |
| A7SRP04REQ | 12’h210 | Shared RAM page04 ownership request semaphore register |
| A7SRP05REQ | 12’h214 | Shared RAM page05 ownership request semaphore register |
| A7SRP06REQ | 12’h218 | Shared RAM page06 ownership request semaphore register |
| A7SRP07REQ | 12’h21c | Shared RAM page07 ownership request semaphore register |
| A7SRP08REQ | 12’h220 | Shared RAM page08 ownership request semaphore register |
| A7SRP09REQ | 12’h224 | Shared RAM page09 ownership request semaphore register |
| A7SRP10REQ | 12’h228 | Shared RAM page10 ownership request semaphore register |
| A7SRP11REQ | 12’h22c | Shared RAM page11 ownership request semaphore register |
| A7SRP12REQ | 12’h230 | Shared RAM page12 ownership request semaphore register |
| A7SRP13REQ | 12’h234 | Shared RAM page13 ownership request semaphore register |
| A7SRP14REQ | 12’h238 | Shared RAM page14 ownership request semaphore register |
| A7SRP15REQ | 12’h23c | Shared RAM page15 ownership request semaphore register |
| A7SRP16REQ | 12’h240 | Shared RAM page16 ownership request semaphore register |
| A7SRP17REQ | 12’h244 | Shared RAM page17 ownership request semaphore register |
| A7SRP18REQ | 12’h248 | Shared RAM page18 ownership request semaphore register |
| A7SRP19REQ | 12’h24c | Shared RAM page19 ownership request semaphore register |
| A7SRP20REQ | 12’h250 | Shared RAM page20 ownership request semaphore register |
| A7SRP21REQ | 12’h254 | Shared RAM page21 ownership request semaphore register |
| A7SRP22REQ | 12’h258 | Shared RAM page22 ownership request semaphore register |
| A7SRP23REQ | 12’h25c | Shared RAM page23 ownership request semaphore register |
| A7SRP24REQ | 12’h260 | Shared RAM page24 ownership request semaphore register |
| A7SRP25REQ | 12’h264 | Shared RAM page25 ownership request semaphore register |
| A7SRP26REQ | 12’h268 | Shared RAM page26 ownership request semaphore register |
| A7SRP27REQ | 12’h26c | Shared RAM page27 ownership request semaphore register |
| A7SRP28REQ | 12’h270 | Shared RAM page28 ownership request semaphore register |
| A7SRP29REQ | 12’h274 | Shared RAM page29 ownership request semaphore register |
| A7SRP30REQ | 12’h278 | Shared RAM page30 ownership request semaphore register |
| A7SRP31REQ | 12’h27c | Shared RAM page31 ownership request semaphore register |
|  |  |  |

### RFIPC Register memory mapping

|  |  |
| --- | --- |
| AHB Master | AHB Base Address |
| RF DSP AHB | 0x 7240\_0000 |

|  |  |  |
| --- | --- | --- |
| Register Name | Offset | Description |
| A7TORFIPCCOMM | 12’h000 | A7 core to RFDSP core IPC command register |
| A7TORFIPCADDR | 12’h004 | A7 core to RFDSP core IPC address register |
| A7TORFIPCDATA0 | 12’h008 | A7 core to RFDSP core IPC data0 register |
| A7TORFIPCDATA1 | 12’h00c | A7 core to RFDSP core IPC data1 register |
| Reserved | 12’h010~  12’h01c |  |
| RFTOA7IPCCOMM | 12’h020 | RFDSP core to A7 core IPC command register |
| RFTOA7IPCADDR | 12’h024 | RFDSP core to A7 core IPC address register |
| RFTOA7IPCDATA0 | 12’h028 | RFDSP core to A7 core IPC data0 register |
| RFTOA7IPCDATA1 | 12’h02c | RFDSP core to A7 core IPC data1 register |
| RFTOPLCIPCCOMM | 12’h030 | RFDSP core to PLCDSP core IPC command register |
| RFTOPLCIPCADDR | 12’h034 | RFDSP core to PLCDSP core IPC address register |
| RFTOPLCIPCDATA0 | 12’h038 | RFDSP core to PLCDSP core IPC data0 register |
| RFTOPLCIPCDATA1 | 12’h03c | RFDSP core to PLCDSP core IPC data1 register |
| Reserved | 12’h040~  12’h04c |  |
| PLCTORFIPCCOMM | 12’h050 | PLCDSP core to RFDSP core IPC command register |
| PLCTORFIPCADDR | 12’h054 | PLCDSP core to RFDSP core IPC address register |
| PLCTORFIPCDATA0 | 12’h058 | PLCDSP core to RFDSP core IPC data0 register |
| PLCTORFIPCDATA1 | 12’h05c | PLCDSP core to RFDSP core IPC data1 register |
| Reserved | 12’h060~  12’h07c |  |
| IPCTMRSCALER | 12’h080 | Free running 64bit timestamp counter prescaler register. |
| IPCCOUNTERL | 12’h084 | Free running 64bit timestamp counter low register. |
| IPCCOUNTERH | 12’h088 | Free running 64bit timestamp counter high register. |
| IPCTMRCONT | 12’h08c | Free running 64bit timestamp control register. |
| SRMSEL0 | 12’h090 | Shared RAM pages’ ownership (master selection) status register0 |
| SRMSEL1 | 12’h094 | Shared RAM pages’ ownership (master selection) status register1 |
| Reserved | 12’h098~  12’h2fc |  |
| RFTOA7IPCSET | 12’h300 | RFDSP core to A7 core IPC set register |
| RFTOA7IPCCLR | 12’h304 | RFDSP core to A7 core IPC clear register |
| RFTOA7IPCFLG | 12’h308 | RFDSP core to A7 core IPC flags register |
| A7TORFIPCACK | 12’h30c | A7 core to RFDSP core IPC event acknowledge register |
| A7TORFIPCSTS | 12’h310 | A7 core to RFDSP core IPC event status register. |
| RFTOPLCIPCSET | 12’h314 | RFDSP core to PLCDSP core IPC set register |
| RFTOPLCIPCCLR | 12’h318 | RFDSP core to PLCDSP core IPC clear register |
| RFTOPLCIPCFLG | 12’h31c | RFDSP core to PLCDSP core IPC flags register |
| PLCTORFIPCACK | 12’h320 | PLCDSP core to RFDSP core IPC event acknowledge register. |
| PLCTORFIPCSTS | 12’h324 | PLCDSP core to RFDSP core IPC event status register. |
| Reserved | 12’h328~  12’h32c |  |
| A7TORFIPCTEST | 12’h330 | A7 core to RFDSP core IPC set register for testing |
| PLCTORFIPCTEST | 12’h334 | PLCDSP core to RFDSP core IPC set register for testing |
| Reserved | 12’h338~  12’h33c |  |
| A7TORFACK\_INT\_CLR | 12’h340 | A7 core to RFDSP core ACK interrupt clear |
| PLCTORFACK\_INT\_CLR | 12’h344 | PLCDSP core to RFDSP core ACK interrupt clear |
| Reserved | 12’h348~  12’h3fc |  |
| RFSRP00REQ | 12’h400 | Shared RAM page00 ownership request semaphore register |
| RFSRP01REQ | 12’h404 | Shared RAM page01 ownership request semaphore register |
| RFSRP02REQ | 12’h408 | Shared RAM page02 ownership request semaphore register |
| RFSRP03REQ | 12’h40c | Shared RAM page03 ownership request semaphore register |
| RFSRP04REQ | 12’h410 | Shared RAM page04 ownership request semaphore register |
| RFSRP05REQ | 12’h414 | Shared RAM page05 ownership request semaphore register |
| RFSRP06REQ | 12’h418 | Shared RAM page06 ownership request semaphore register |
| RFSRP07REQ | 12’h41c | Shared RAM page07 ownership request semaphore register |
| RFSRP08REQ | 12’h420 | Shared RAM page08 ownership request semaphore register |
| RFSRP09REQ | 12’h424 | Shared RAM page09 ownership request semaphore register |
| RFSRP10REQ | 12’h428 | Shared RAM page10 ownership request semaphore register |
| RFSRP11REQ | 12’h42c | Shared RAM page11 ownership request semaphore register |
| RFSRP12REQ | 12’h430 | Shared RAM page12 ownership request semaphore register |
| RFSRP13REQ | 12’h434 | Shared RAM page13 ownership request semaphore register |
| RFSRP14REQ | 12’h438 | Shared RAM page14 ownership request semaphore register |
| RFSRP15REQ | 12’h43c | Shared RAM page15 ownership request semaphore register |
| RFSRP16REQ | 12’h440 | Shared RAM page16 ownership request semaphore register |
| RFSRP17REQ | 12’h444 | Shared RAM page17 ownership request semaphore register |
| RFSRP18REQ | 12’h448 | Shared RAM page18 ownership request semaphore register |
| RFSRP19REQ | 12’h44c | Shared RAM page19 ownership request semaphore register |
| RFSRP20REQ | 12’h450 | Shared RAM page20 ownership request semaphore register |
| RFSRP21REQ | 12’h454 | Shared RAM page21 ownership request semaphore register |
| RFSRP22REQ | 12’h458 | Shared RAM page22 ownership request semaphore register |
| RFSRP23REQ | 12’h45c | Shared RAM page23 ownership request semaphore register |
| RFSRP24REQ | 12’h460 | Shared RAM page24 ownership request semaphore register |
| RFSRP25REQ | 12’h464 | Shared RAM page25 ownership request semaphore register |
| RFSRP26REQ | 12’h468 | Shared RAM page26 ownership request semaphore register |
| RFSRP27REQ | 12’h46c | Shared RAM page27 ownership request semaphore register |
| RFSRP28REQ | 12’h470 | Shared RAM page28 ownership request semaphore register |
| RFSRP29REQ | 12’h474 | Shared RAM page29 ownership request semaphore register |
| RFSRP30REQ | 12’h478 | Shared RAM page30 ownership request semaphore register |
| RFSRP31REQ | 12’h47c | Shared RAM page31 ownership request semaphore register |
|  |  |  |

### PLCIPC Register memory mapping

|  |  |
| --- | --- |
| AHB Master | AHB Base Address |
| PLC DSP AHB | 0x6150\_0000 |

|  |  |  |
| --- | --- | --- |
| Register Name | Offset | Description |
| Reserved | 12’h000~  12’h00c |  |
| A7TOPLCIPCCOMM | 12’h010 | A7 core to PLCDSP core IPC command register |
| A7TOPLCIPCADDR | 12’h014 | A7 core to PLCDSP core IPC address register |
| A7TOPLCIPCDATA0 | 12’h018 | A7 core to PLCDSP core IPC data0 register |
| A7TOPLCIPCDATA1 | 12’h01c | A7 core to PLCDSP core IPC data1 register |
| Reserved | 12’h020~  12’h02c |  |
| RFTOPLCIPCCOMM | 12’h030 | RFDSP core to PLCDSP core IPC command register |
| RFTOPLCIPCADDR | 12’h034 | RFDSP core to PLCDSP core IPC address register |
| RFTOPLCIPCDATA0 | 12’h038 | RFDSP core to PLCDSP core IPC data0 register |
| RFTOPLCIPCDATA1 | 12’h03c | RFDSP core to PLCDSP core IPC data1 register |
| PLCTOA7IPCCOMM | 12’h040 | PLCDSP core to A7 core IPC command register |
| PLCTOA7IPCADDR | 12’h044 | PLCDSP core to A7 core IPC address register |
| PLCTOA7IPCDATA0 | 12’h048 | PLCDSP core to A7 core IPC data0 register |
| PLCTOA7IPCDATA1 | 12’h04c | PLCDSP core to A7 core IPC data1 register |
| PLCTORFIPCCOMM | 12’h050 | PLCDSP core to RFDSP core IPC command register |
| PLCTORFIPCADDR | 12’h054 | PLCDSP core to RFDSP core IPC address register |
| PLCTORFIPCDATA0 | 12’h058 | PLCDSP core to RFDSP core IPC data0 register |
| PLCTORFIPCDATA1 | 12’h05c | PLCDSP core to RFDSP core IPC data1 register |
| Reserved | 12’h058~  12’h07c |  |
| IPCTMRSCALER | 12’h080 | Free running 64bit timestamp counter prescaler register. |
| IPCCOUNTERL | 12’h084 | Free running 64bit timestamp counter low register. |
| IPCCOUNTERH | 12’h088 | Free running 64bit timestamp counter high register. |
| IPCTMRCONT | 12’h08c | Free running 64bit timestamp control register. |
| SRMSEL0 | 12’h090 | Shared RAM pages’ ownership (master selection) status register0 |
| SRMSEL1 | 12’h094 | Shared RAM pages’ ownership (master selection) status register1 |
| Reserved | 12’h098~  12’h4fc |  |
| PLCTOA7IPCSET | 12’h500 | PLCDSP core to A7 core IPC set register |
| PLCTOA7IPCCLR | 12’h504 | PLCDSP core to A7 core IPC clear register |
| PLCTOA7IPCFLG | 12’h508 | PLCDSP core to A7 core IPC flags register |
| A7TOPLCIPCACK | 12’h50c | A7 core to PLCDSP core IPC event acknowledge register. |
| A7TOPLCIPCSTS | 12’h510 | A7 core to PLCDSP core IPC event status register. |
| PLCTORFIPCSET | 12’h514 | PLCDSP core to RFDSP core IPC set register |
| PLCTORFIPCCLR | 12’h518 | PLCDSP core to RFDSP core IPC event clear register |
| PLCTORFIPCFLG | 12’h51c | PLCDSP core to RFDSP core IPC flags register |
| RFTOPLCIPCACK | 12’h520 | PLCDSP core to A7 core IPC event acknowledge register. |
| RFTOPLCIPCSTS | 12’h524 | PLCDSP core to A7 core IPC event status register. |
| A7TOPLCIPCTEST | 12’h530 | A7 core to PLCDSP core IPC set register for testing |
| RFTOPLCIPCTEST | 12’h534 | RFDSP core to PLCDSP core IPC set register for testing |
| Reserved | 12’h538~  12’h53c |  |
| A7TOPLCACK\_INT\_CLR | 12’h540 | A7 core to PLCDSP core ACK interrupt clear |
| RFTOPLCACK\_INT\_CLR | 12’h544 | RFDSP core to PLCDSP core ACK interrupt clear |
| Reserved | 12’h548~  12’h5fc |  |
|  |  |  |
| PLCSRP00REQ | 12’h600 | Shared RAM page00 ownership request semaphore register |
| PLCSRP01REQ | 12’h604 | Shared RAM page01 ownership request semaphore register |
| PLCSRP02REQ | 12’h608 | Shared RAM page02 ownership request semaphore register |
| PLCSRP03REQ | 12’h60c | Shared RAM page03 ownership request semaphore register |
| PLCSRP04REQ | 12’h610 | Shared RAM page04 ownership request semaphore register |
| PLCSRP05REQ | 12’h614 | Shared RAM page05 ownership request semaphore register |
| PLCSRP06REQ | 12’h618 | Shared RAM page06 ownership request semaphore register |
| PLCSRP07REQ | 12’h61c | Shared RAM page07 ownership request semaphore register |
| PLCSRP08REQ | 12’h620 | Shared RAM page08 ownership request semaphore register |
| PLCSRP09REQ | 12’h624 | Shared RAM page09 ownership request semaphore register |
| PLCSRP10REQ | 12’h628 | Shared RAM page10 ownership request semaphore register |
| PLCSRP11REQ | 12’h62c | Shared RAM page11 ownership request semaphore register |
| PLCSRP12REQ | 12’h630 | Shared RAM page12 ownership request semaphore register |
| PLCSRP13REQ | 12’h634 | Shared RAM page13 ownership request semaphore register |
| PLCSRP14REQ | 12’h638 | Shared RAM page14 ownership request semaphore register |
| PLCSRP15REQ | 12’h63c | Shared RAM page15 ownership request semaphore register |
| PLCSRP16REQ | 12’h640 | Shared RAM page16 ownership request semaphore register |
| PLCSRP17REQ | 12’h644 | Shared RAM page17 ownership request semaphore register |
| PLCSRP18REQ | 12’h648 | Shared RAM page18 ownership request semaphore register |
| PLCSRP19REQ | 12’h64c | Shared RAM page19 ownership request semaphore register |
| PLCSRP20REQ | 12’h650 | Shared RAM page20 ownership request semaphore register |
| PLCSRP21REQ | 12’h654 | Shared RAM page21 ownership request semaphore register |
| PLCSRP22REQ | 12’h658 | Shared RAM page22 ownership request semaphore register |
| PLCSRP23REQ | 12’h65c | Shared RAM page23 ownership request semaphore register |
| PLCSRP24REQ | 12’h660 | Shared RAM page24 ownership request semaphore register |
| PLCSRP25REQ | 12’h664 | Shared RAM page25 ownership request semaphore register |
| PLCSRP26REQ | 12’h668 | Shared RAM page26 ownership request semaphore register |
| PLCSRP27REQ | 12’h66c | Shared RAM page27 ownership request semaphore register |
| PLCSRP28REQ | 12’h670 | Shared RAM page28 ownership request semaphore register |
| PLCSRP29REQ | 12’h674 | Shared RAM page29 ownership request semaphore register |
| PLCSRP30REQ | 12’h678 | Shared RAM page30 ownership request semaphore register |
| PLCSRP31REQ | 12’h67c | Shared RAM page31 ownership request semaphore register |
|  |  |  |

### ShareRAM Register memory mapping

|  |  |
| --- | --- |
| AHB Master | AHB Base Address |
| A7 AHB | 0xC260\_0000 |
| RF DSP AHB | 0x7260\_0000 |
| PLC DSP AHB | 0x 6160\_0000 |

### ARM Subsystem IPC registers

### A7TORFIPCCOMM<31:0>

A7 core to RFDSP core IPC command register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | COMMAND | R/W | 0 | This is a general purpose register used to send software-defined commands from A7 to RFDSP. |

### A7TORFIPCADDR<31:0>

A7 core to RFDSP core IPC address register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | ADDRESS | R/W | 0 | This is a general purpose register used to send software-defined address from A7 to RFDSP. |

### A7TORFIPCDATA0<31:0>

A7 core to RFDSP core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA0 | R/W | 0 | This is a general purpose register used to send software-defined data from A7 to RFDSP. |

### A7TORFIPCDATA1<31:0>

A7 core to RFDSP core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA1 | R/W | 0 | This is a general purpose register used to send software-defined data from A7 to RFDSP. |

### A7TOPLCIPCCOMM<31:0>

A7 core to PLCDSP core IPC command register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | COMMAND | R/W | 0 | This is a general purpose register used to send software-defined commands from A7 to PLCDSP. |

### A7TOPLCIPCADDR<31:0>

A7 core to PLCDSP core IPC address register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | ADDRESS | R/W | 0 | This is a general purpose register used to send software-defined address from A7 to PLCDSP. |

### A7TOPLCIPCDATA0<31:0>

A7 core to PLCDSP core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA0 | R/W | 0 | This is a general purpose register used to send software-defined data from A7 to PLCDSP. |

### A7TOPLCIPCDATA1<31:0>

A7 core to PLCDSP core IPC response register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA1 | R/W | 0 | This is a general purpose register used to sendsoftware-defined data from A7 to PLCDSP. |

### RFTOA7IPCCOMM<31:0>

RFDSP core to A7 core IPC command register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | COMMAND | R | 0 | This is a general purpose register used to send software-defined commands from RFDSP to A7. |

### RFTOA7IPCADDR<31:0>

RFDSP core to A7 core IPC address register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | ADDRESS | R | 0 | This is a general purpose register used to send software-defined address from RFDSP to A7. |

### RFTOA7IPCDATA0<31:0>

RFDSP core to A7 core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA0 | R | 0 | This is a general purpose register used to send software-defined data from RFDSP to A7. |

### RFTOA7IPCDATA1<31:0>

RFDSP core to A7 core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA1 | R | 0 | This is a general purpose register used to to send software-defined data from RFDSP to A7. |

### PLCTOA7IPCCOMM<31:0>

PLCDSP core to A7 core IPC command register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | COMMAND | R | 0 | This is a general purpose register used to send software-defined commands from PLCDSP to A7. |

### PLCTOA7IPCADDR<31:0>

PLCDSP core to A7 core IPC address register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | ADDRESS | R | 0 | This is a general purpose register used to send software-defined address from PLCDSP to A7. |

### PLCTOA7IPCDATA0<31:0>

PLCDSP core to A7 core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA0 | R | 0 | This is a general purpose register used to send software-defined data from PLCDSP to A7. |

### PLCTOA7IPCDATA1<31:0>

PLCDSP core to A7 core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA1 | R | 0 | This is a general purpose register used to send software-defined data from PLCDSP to A7. |

### IPCTMRSCALER <31:0>

Free running 64bit timestamp counter prescaler register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15:0 | PRESCALER | R | 0 | The prescaler value used to derive the free running timer’s clock: Ftimer=Fcpu/(prescaler+1).  Prescale counter is reset whenever this setting or IPCTMRCNT is changed  It can be only configured by RF Core |

### IPCCOUNTERL <31:0>

Free running 64bit timestamp counter low register.

To ensure the integrity of read data from AHB bus, a snapshot for the high 32-bits counter is taken when a read is performed on the IPCCOUNTERL register. When the A7 core reads the IPCOUNTERH, the snapshot is fed back to the user instead of the current value in the IPCOUNTERH register. Therefore, the user application software must always read IPCCOUNTERL first and then read IPCCOUNTERH.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | IPCCOUNTERL | R | 0 | This is the lower 32-bits of free running 64 bit timestamp counter clocked by the divided clock. |

### IPCCOUNTERH <31:0>

Free running 64bit timestamp counter high register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | IPCCOUNTERH | R | 0 | This is the upper 32-bits of free running 64 bit timestamp counter clocked by the divided clock. |

### IPCTMRCONT <31:0>

Free running 64bit control register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:1 | Reserved |  |  |  |
| 0 | TMRCOUNTUP | R | 1 | 0x1: Timer as upward counter  0x0: Timer as downward counter  It can be only configured by RF Core  Timer count value is reset to 0x0 (count up) or 0xffffffff\_ffffffff (count down) whenever TMRCOUNTUP setting is changed |

### SRMSEL0<31:0>

Shared RAM pages’ ownership (master selection) status register0

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:30 | SRP15OWN | R | 0 | Shared RAM page15 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 29:28 | SRP14OWN | R | 0 | Shared RAM page 14 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 27:26 | SRP13OWN | R | 0 | Shared RAM page 13 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 25:24 | SRP12OWN | R | 0 | Shared RAM page 12 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 23:22 | SRP110OWN | R | 0 | Shared RAM page 11 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 21:20 | SRP10OWN | R | 0 | Shared RAM page 10 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 19:18 | SRP09OWN | R | 0 | Shared RAM page 9 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 17:16 | SRP08OWN | R | 0 | Shared RAM page 8 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 15:14 | SRP07OWN | R | 0 | Shared RAM page 7 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 13:12 | SRP06OWN | R | 0 | Shared RAM page 6 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 11:10 | SRP05OWN | R | 0 | Shared RAM page 5 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 9:8 | SRP04OWN | R | 0 | Shared RAM page 4 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 7:6 | SRP03OWN | R | 0 | Shared RAM page 3 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 5:4 | SRP02OWN | R | 0 | Shared RAM page 2 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 3:2 | SRP01OWN | R | 0 | Shared RAM page 1 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 1:0 | SRP00OWN | R | 0 | Shared RAM page 0 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |

### SRMSEL1<31:0>

Shared RAM pages’ ownership (master selection) status register1

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:30 | SRP31OWN | R | 0 | Shared RAM page 31 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 29:28 | SRP30OWN | R | 0 | Shared RAM page 30 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 27:26 | SRP29OWN | R | 0 | Shared RAM page 29 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 25:24 | SRP28OWN | R | 0 | Shared RAM page 28 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 23:22 | SRP270OWN | R | 0 | Shared RAM page 27 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 21:20 | SRP26OWN | R | 0 | Shared RAM page 26 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 19:18 | SRP25OWN | R | 0 | Shared RAM page 25 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 17:16 | SRP24OWN | R | 0 | Shared RAM page 24 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 15:14 | SRP23OWN | R | 0 | Shared RAM page 23 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 13:12 | SRP22OWN | R | 0 | Shared RAM page 22 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 11:10 | SRP21OWN | R | 0 | Shared RAM page 21 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 9:8 | SRP20OWN | R | 0 | Shared RAM page 20 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 7:6 | SRP19OWN | R | 0 | Shared RAM page 19 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 5:4 | SRP18OWN | R | 0 | Shared RAM page 18 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 3:2 | SRP17OWN | R | 0 | Shared RAM page 17 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 1:0 | SRP16OWN | R | 0 | Shared RAM page 16 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |

### A7TORFIPCSET<15:0>

A7 core to RFDSP core IPC set register

Address Offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | A7TORFIPCSET<15> | W | 0 | A7 to RFDSP core IPC flag 15 set.  Writing 1 to this bit sets the A7TORFIPCFLG<15> for the A7 and A7TORFIPCSTS<15> for the RFDSP.  Writing 0 has no effect. |
| 14 | A7TORFIPCSET<14> | W | 0 | A7 to RFDSP core IPC flag 14 set.  Writing 1 to this bit sets the A7TORFIPCFLG<14> for the A7 and A7TORFIPCSTS<14> for the RFDSP.  Writing 0 has no effect. |
| 13 | A7TORFIPCSET<13> | W | 0 | A7 to RFDSP core IPC flag 13 set.  Writing 1 to this bit sets the A7TORFIPCFLG<13> for the A7 and A7TORFIPCSTS<13> for the RFDSP.  Writing 0 has no effect. |
| 12 | A7TORFIPCSET<12> | W | 0 | A7 to RFDSP core IPC flag 12 set.  Writing 1 to this bit sets the A7TORFIPCFLG<12> for the A7 and A7TORFIPCSTS<12> for the RFDSP.  Writing 0 has no effect. |
| 11 | A7TORFIPCSET<11> | W | 0 | A7 to RFDSP core IPC flag 11 set.  Writing 1 to this bit sets the A7TORFIPCFLG<11> for the A7 and A7TORFIPCSTS<11> for the RF DSP.  Writing 0 has no effect. |
| 10 | A7TORFIPCSET<10> | W | 0 | A7 to RFDSP core IPC flag 10 set.  Writing 1 to this bit sets the A7TORFIPCFLG<10> for the A7 and A7TORFIPCSTS<10> for the RFDSP.  Writing 0 has no effect. |
| 9 | A7TORFIPCSET<9 | W | 0 | A7 to RFDSP core IPC flag 9 set.  Writing 1 to this bit sets the A7TORFIPCFLG<9> for the A7 and A7TORFIPCSTS<9> for the RFDSP.  Writing 0 has no effect. |
| 8 | A7TORFIPCSET<8> | W | 0 | A7 to RFDSP core IPC flag 8 set.  Writing 1 to this bit sets the A7TORFIPCFLG<8> for the A7 and A7TORFIPCSTS<8> for the RF DSP.  Writing 0 has no effect. |
| 7 | A7TORFIPCSET<7> | W | 0 | A7 to RFDSP core IPC flag 7 set.  Writing 1 to this bit sets the A7TORFIPCFLG<7> for the A7 and A7TORFIPCSTS<7> for the RFDSP.  Writing 0 has no effect. |
| 6 | A7TORFIPCSET<6> | W | 0 | A7 to RFDSP core IPC flag 6 set.  Writing 1 to this bit sets the A7TORFIPCFLG<6> for the A7 and A7TORFIPCSTS<6> for the RFDSP.  Writing 0 has no effect. |
| 5 | A7TORFIPCSET<5> | W | 0 | A7 to RFDSP core IPC flag 5 set.  Writing 1 to this bit sets the A7TORFIPCFLG<5> for the A7 and A7TORFIPCSTS<5> for the RFDSP.  Writing 0 has no effect. |
| 4 | A7TORFIPCSET<4> | W | 0 | A7 to RFDSP core IPC flag 4 set.  Writing 1 to this bit sets the A7TORFIPCFLG<4> for the A7 and A7TORFIPCSTS<4> for the RFDSP.  Writing 0 has no effect. |
| 3 | A7TORFIPCSET<3> | W | 0 | A7 to RFDSP core IPC flag 3 set.  Writing 1 to this bit sets the A7TORFIPCFLG<3> for the A7 and A7TORFIPCSTS<3> for the RFDSP  Writing 0 has no effect. |
| 2 | A7TORFIPCSET<2> | W | 0 | A7 to RFDSP core IPC flag 2 set.  Writing 1 to this bit sets the A7TORFIPCFLG<2> for the A7 and A7TORFIPCSTS<2> for the RFDSP.  Writing 0 has no effect. |
| 1 | A7TORFIPCSET<1> | W | 0 | A7 to RFDSP core IPC flag 1 set.  Writing 1 to this bit sets the A7TORFIPCFLG<1> for the A7 and A7TORFIPCSTS<1> for the RFDSP.  Writing 0 has no effect. |
| 0 | A7TORFIPCSET<0> | W | 0 | A7 to RFDSP core IPC flag 0 set.  Writing 1 to this bit sets the A7TORFIPCFLG<0> for the A7 and A7TORFIPCSTS<0> for the RFDSP.  Writing 0 has no effect. |

### A7TORFIPCCLR<15:0>

A7 core to RFDSP core IPC clear register

Address Offset

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | A7TORFIPCCLR<15> | W | 0 | A7 to RFDSP core IPC flag 15 clear.  Writing 1 to this bit clears the A7TORFIPCFLG<15> for the A7 and A7TORFIPCSTS<15> for the RFDSP.  Writing 0 has no effect. |
| 14 | A7TORFIPCCLR<14> | W | 0 | A7 to RFDSP core IPC flag 14 clear.  Writing 1 to this bit clears the A7TORFIPCFLG<14> for the A7 and A7TORFIPCSTS<14> for the RFDSP.  Writing 0 has no effect. |
| 13 | A7TORFIPCCLR<13> | W | 0 | A7 to RFDSP core IPC flag 13 clear.  Writing 1 to this bit clears the A7TORFIPCFLG<13> for the A7 and A7TORFIPCSTS<13> for the RFDSP.  Writing 0 has no effect. |
| 12 | A7TORFIPCCLR<12> | W | 0 | A7 to RFDSP core IPC flag 12 clear.  Writing 1 to this bit clears the A7TORFIPCFLG<12> for the A7 and A7TORFIPCSTS<12> for the RFDSP.  Writing 0 has no effect. |
| 11 | A7TORFIPCCLR<11> | W | 0 | A7 to RFDSP core IPC flag 11 clear.  Writing 1 to this bit clears the A7TORFIPCFLG<11> for the A7 and A7TORFIPCSTS<11> for the RFDSP.  Writing 0 has no effect. |
| 10 | A7TORFIPCCLR<10> | W | 0 | A7 to RFDSP core IPC flag 10 clear.  Writing 1 to this bit clears the A7TORFIPCFLG<10> for the A7 and A7TORFIPCSTS<10> for the RFDSP.  Writing 0 has no effect. |
| 9 | A7TORFIPCCLR<9> | W | 0 | A7 to RFDSP core IPC flag 9 clear.  Writing 1 to this bit clears the A7TORFIPCFLG<9> for the A7 and A7TORFIPCSTS<9> for the RFDSP.  Writing 0 has no effect. |
| 8 | A7TORFIPCCLR<8> | W | 0 | A7 to RFDSP core IPC flag 8 clear.  Writing 1 to this bit clears the A7TORFIPCFLG<8> for the A7 and A7TORFIPCSTS<8> for the RFDSP.  Writing 0 has no effect. |
| 7 | A7TORFIPCCLR<7> | W | 0 | A7 to RFDSP core IPC flag 7 clear.  Writing 1 to this bit clears the A7TORFIPCFLG<7> for the A7 and A7TORFIPCSTS<7> for the RFDSP.  Writing 0 has no effect. |
| 6 | A7TORFIPCCLR<6> | W | 0 | A7 to RFDSP core IPC flag 6 clear.  Writing 1 to this bit clears the A7TORFIPCFLG<6> for the A7 and A7TORFIPCSTS<6> for the RFDSP.  Writing 0 has no effect. |
| 5 | A7TORFIPCCLR<5> | W | 0 | A7 to RFDSP core IPC flag 5 clear.  Writing 1 to this bit clears the A7TORFIPCFLG<5> for the A7 and A7TORFIPCSTS<5> for the RFDSP.  Writing 0 has no effect. |
| 4 | A7TORFIPCCLR<4> | W | 0 | A7 to RFDSP core IPC flag 4 clear.  Writing 1 to this bit clears the A7TORFIPCFLG<4> for the A7 and A7TORFIPCSTS<4> for the RFDSP.  Writing 0 has no effect. |
| 3 | A7TORFIPCCLR<3> | W | 0 | A7 to RFDSP core IPC flag 3 clear.  Writing 1 to this bit clears the A7TORFIPCFLG<3> for the A7 and A7TORFIPCSTS<3> for the RFDSP.  Writing 0 has no effect. |
| 2 | A7TORFIPCCLR<2> | W | 0 | A7 to RFDSP core IPC flag 2 clear.  Writing 1 to this bit clears the A7TORFIPCFLG<2> for the A7 and A7TORFIPCSTS<2> for the RFDSP.  Writing 0 has no effect. |
| 1 | A7TORFIPCCLR<1> | W | 0 | A7 to RFDSP core IPC flag 1 clear.  Writing 1 to this bit clears the A7TORFIPCFLG<1> for the A7 and A7TORFIPCSTS<1> for the RFDSP.  Writing 0 has no effect. |
| 0 | A7TORFIPCCLR<0> | W | 0 | A7 to RFDSP core IPC flag 0 clear.  Writing 1 to this bit clears the A7TORFIPCFLG<0> for the A7 and A7TORFIPCSTS<0> for the RFDSP.  Writing 0 has no effect. |

Notes: Normally, RFDSP will clear (acknowledge) the A7toRF IPC event flags. This mechanism may be useful if RF DSP is non-responsive.

### A7TORFIPCFLG<15:0>

A7 core to RFDSP core IPC flags register

Address Offset

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | A7TORFIPCFLG<15> | R | 0 | A7 to RFDSP core IPC flag 15 status.  Indicates to A7 whether theA7TORF IPCFLG<15> is set.  0: The event flag is not set  1: The event flag is set |
| 14 | A7TORFIPCFLG<14> | R | 0 | A7 to RFDSP core IPC flag 14 status.  Indicates to A7 whether theA7TORF IPCFLG<14> is set.  0: The event flag is not set  1: The event flag is set |
| 13 | A7TORFIPCFLG<13> | R | 0 | A7 to RFDSP core IPC flag 13 status.  Indicates to A7 whether theA7TORF IPCFLG<13> is set.  0: The event flag is not set  1: The event flag is set |
| 12 | A7TORFIPCFLG<12> | R | 0 | A7 to RFDSP core IPC flag 12 status.  Indicates to A7 whether theA7TORF IPCFLG<12> is set.  0: The event flag is not set  1: The event flag is set |
| 11 | A7TORFIPCFLG<11> | R | 0 | A7 to RFDSP core IPC flag 11 status.  Indicates to A7 whether theA7TORF IPCFLG<11> is set.  0: The event flag is not set  1: The event flag is set |
| 10 | A7TORFIPCFLG<10> | R | 0 | A7 to RFDSP core IPC flag 10 status.  Indicates to A7 whether theA7TORF IPCFLG<10> is set.  0: The event flag is not set  1: The event flag is set |
| 9 | A7TORFIPCFLG<9 | R | 0 | A7 to RFDSP core IPC flag 9 status.  Indicates to A7 whether theA7TORF IPCFLG<9> is set.  0: The event flag is not set  1: The event flag is set |
| 8 | A7TORFIPCFLG<8> | R | 0 | A7 to RFDSP core IPC flag 8 status.  Indicates to A7 whether theA7TORF IPCFLG<8> is set.  0: The event flag is not set  1: The event flag is set |
| 7 | A7TORFIPCFLG<7> | R | 0 | A7 to RFDSP core IPC flag 7 status.  Indicates to A7 whether theA7TORF IPCFLG<7> is set.  0: The event flag is not set  1: The event flag is set |
| 6 | A7TORFIPCFLG<6> | R | 0 | A7 to RFDSP core IPC flag 6 status.  Indicates to A7 whether theA7TORF IPCFLG<6> is set.  0: The event flag is not set  1: The event flag is set |
| 5 | A7TORFIPCFLG<5> | R | 0 | A7 to RFDSP core IPC flag 5 status.  Indicates to A7 whether theA7TORF IPCFLG<5> is set.  0: The event flag is not set  1: The event flag is set |
| 4 | A7TORFIPCFLG<4> | R | 0 | A7 to RFDSP core IPC flag 4 status.  Indicates to A7 whether theA7TORF IPCFLG<4> is set.  0: The event flag is not set  1: The event flag is set |
| 3 | A7TORFIPCFLG<3> | R | 0 | A7 to RFDSP core IPC flag 3 status.  Indicates to A7 whether theA7TORF IPCFLG<3> is set.  0: The event flag is not set  1: The event flag is set |
| 2 | A7TORFIPCFLG<2> | R | 0 | A7 to RFDSP core IPC flag 2 status.  Indicates to A7 whether theA7TORF IPCFLG<2> is set.  0: The event flag is not set  1: The event flag is set |
| 1 | A7TORFIPCFLG<1> | R | 0 | A7 to RFDSP core IPC flag 1 status.  Indicates to A7 whether theA7TORF IPCFLG<1> is set.  0: The event flag is not set  1: The event flag is set |
| 0 | A7TORFIPCFLG<0> | R | 0 | A7 to RFDSP core IPC flag 0 status.  Indicates to A7 whether theA7TORF IPCFLG<0> is set.  0: The event flag is not set  1: The event flag is set |

### RFTOA7IPCACK<15:0>

RFDSP core to A7 core IPC event acknowledge register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | RFTOA7IPCACK<15> | W | 0 | RFDSP to A7 IPC event 15 acknowledge.  Writing 1 to this bit clears the RFTOA7IPCFLG<15> and RFTOA7IPCSTS<15> which are set by RFDSP.  Writing 0 to this bit has no effect |
| 14 | RFTOA7IPCACK<14> | W | 0 | RFDSP to A7 IPC event 14 acknowledge.  Writing 1 to this bit clears the RFTOA7IPCFLG<14> and RFTOA7IPCSTS<14> which are set by RFDSP.  Writing 0 to this bit has no effect |
| 13 | RFTOA7IPCACK<13> | W | 0 | RFDSP to A7 IPC event 13 acknowledge.  Writing 1 to this bit clears the RFTOA7IPCFLG<13> and RFTOA7IPCSTS<13> which are set by RFDSP.  Writing 0 to this bit has no effect |
| 12 | RFTOA7IPCACK<12> | W | 0 | RFDSP to A7 IPC event 12 acknowledge.  Writing 1 to this bit clears the RFTOA7IPCFLG<12> and RFTOA7IPCSTS<12> which are set by RFDSP.  Writing 0 to this bit has no effect |
| 11 | RFTOA7IPCACK<11> | W | 0 | RFDSP to A7 IPC event 11 acknowledge.  Writing 1 to this bit clears the RFTOA7IPCFLG<11> and RFTOA7IPCSTS<11> which are set by RFDSP.  Writing 0 to this bit has no effect |
| 10 | RFTOA7IPCACK<10> | W | 0 | RFDSP to A7 IPC event 10 acknowledge.  Writing 1 to this bit clears the RFTOA7IPCFLG<10> and RFTOA7IPCSTS<10> which are set by RFDSP.  Writing 0 to this bit has no effect |
| 9 | RFTOA7IPCACK<9 | W | 0 | RFDSP to A7 IPC event 9 acknowledge.  Writing 1 to this bit clears the RFTOA7IPCFLG<9> and RFTOA7IPCSTS<9> which are set by RFDSP.  Writing 0 to this bit has no effect |
| 8 | RFTOA7IPCACK<8> | W | 0 | RFDSP to A7 IPC event 8 acknowledge.  Writing 1 to this bit clears the RFTOA7IPCFLG<8> and RFTOA7IPCSTS<8> which are set by RFDSP.  Writing 0 to this bit has no effect |
| 7 | RFTOA7IPCACK<7> | W | 0 | RFDSP to A7 IPC event 7 acknowledge.  Writing 1 to this bit clears the RFTOA7IPCFLG<7> and RFTOA7IPCSTS<7> which are set by RFDSP.  Writing 0 to this bit has no effect |
| 6 | RFTOA7IPCACK<6> | W | 0 | RFDSP to A7 IPC event 6 acknowledge.  Writing 1 to this bit clears the RFTOA7IPCFLG<6> and RFTOA7IPCSTS<6> which are set by RFDSP.  Writing 0 to this bit has no effect |
| 5 | RFTOA7IPCACK<5> | W | 0 | RFDSP to A7 IPC event 5 acknowledge.  Writing 1 to this bit clears the RFTOA7IPCFLG<5> and RFTOA7IPCSTS<5> which are set by RFDSP.  Writing 0 to this bit has no effect |
| 4 | RFTOA7IPCACK<4> | W | 0 | RFDSP to A7 IPC event 4 acknowledge.  Writing 1 to this bit clears the RFTOA7IPCFLG<4> and RFTOA7IPCSTS<4> which are set by RFDSP.  Writing 0 to this bit has no effect |
| 3 | RFTOA7IPCACK<3> | W | 0 | RFDSP to A7 IPC event 3 acknowledge.  Writing 1 to this bit clears the RFTOA7IPCFLG<3> and RFTOA7IPCSTS<3> which are set by RFDSP.  Writing 0 to this bit has no effect |
| 2 | RFTOA7IPCACK<2> | W | 0 | RFDSP to A7 IPC event 2 acknowledge.  Writing 1 to this bit clears the RFTOA7IPCFLG<2> and RFTOA7IPCSTS<2> which are set by RFDSP.  Writing 0 to this bit has no effect |
| 1 | RFTOA7IPCACK<1> | W | 0 | RFDSP to A7 IPC event 1 acknowledge.  Writing 1 to this bit clears the RFTOA7IPCFLG<1> and RFTOA7IPCSTS<1> which are set by RFDSP.  Writing 0 to this bit has no effect |
| 0 | RFTOA7IPCACK<0> | W | 0 | RFDSP to A7 IPC event 0 acknowledge.  Writing 1 to this bit clears the RFTOA7IPCFLG<0> and RFTOA7IPCSTS<0> which are set by RFDSP.  Writing 0 to this bit has no effect |

### RFTOA7IPCSTS<15:0>

RFDSP core to A7 core IPC event status register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | RFTOA7IPCSTS<15> | R | 0 | RFDSP to A7 core IPC event 15 status.  Indicates to A7 whether the RFTOA7IPC event 15 is set or not by RFDSP.  0: No event is set by RFDSP  1: An event is set by RFDSP |
| 14 | RFTOA7IPCSTS<14> | R | 0 | RFDSP to A7 core IPC event 14 status.  Indicates to A7 whether the RFTOA7IPC event 14 is set or not by RFDSP.  0: No event is set by RFDSP  1: An event is set by RFDSP |
| 13 | RFTOA7IPCSTS<13> | R | 0 | RFDSP to A7 core IPC event 13 status.  Indicates to A7 whether the RFTOA7IPC event 13 is set or not by RFDSP.  0: No event is set by RFDSP  1: An event is set by RFDSP |
| 12 | RFTOA7IPCSTS<12> | R | 0 | RFDSP to A7 core IPC event 12 status.  Indicates to A7 whether the RFTOA7IPC event 12 is set or not by RFDSP.  0: No event is set by RFDSP  1: An event is set by RFDSP |
| 11 | RFTOA7IPCSTS<11> | R | 0 | RFDSP to A7 core IPC event 11 status.  Indicates to A7 whether the RFTOA7IPC event 11 is set or not by RFDSP.  0: No event is set by RFDSP  1: An event is set by RFDSP |
| 10 | RFTOA7IPCSTS<10> | R | 0 | RFDSP to A7 core IPC event 10 status.  Indicates to A7 whether the RFTOA7IPC event 10 is set or not by RFDSP.  0: No event is set by RFDSP  1: An event is set by RFDSP |
| 9 | RFTOA7IPCSTS<9 | R | 0 | RFDSP to A7 core IPC event 9 status.  Indicates to A7 whether the RFTOA7IPC event 9 is set or not by RFDSP.  0: No event is set by RFDSP  1: An event is set by RFDSP |
| 8 | RFTOA7IPCSTS<8> | R | 0 | RFDSP to A7 core IPC event 8 status.  Indicates to A7 whether the RFTOA7IPC event 8 is set or not by RFDSP.  0: No event is set by RFDSP  1: An event is set by RFDSP |
| 7 | RFTOA7IPCSTS<7> | R | 0 | RFDSP to A7 core IPC event 7 status.  Indicates to A7 whether the RFTOA7IPC event 7 is set or not by RFDSP.  0: No event is set by RFDSP  1: An event is set by RFDSP |
| 6 | RFTOA7IPCSTS<6> | R | 0 | RFDSP to A7 core IPC event 6 status.  Indicates to A7 whether the RFTOA7IPC event 6 is set or not by RFDSP.  0: No event is set by RFDSP  1: An event is set by RFDSP |
| 5 | RFTOA7IPCSTS<5> | R | 0 | RFDSP to A7 core IPC event 5 status.  Indicates to A7 whether the RFTOA7IPC event 5 is set or not by RFDSP.  0: No event is set by RFDSP  1: An event is set by RFDSP |
| 4 | RFTOA7IPCSTS<4> | R | 0 | RFDSP to A7 core IPC event 4 status.  Indicates to A7 whether the RFTOA7IPC event 4 is set or not by RFDSP.  0: No event is set by RFDSP  1: An event is set by RFDSP |
| 3 | RFTOA7IPCSTS<3> | R | 0 | RFDSP to A7 core IPC event 3 status.  Indicates to A7 whether the RFTOA7IPC event 3 is set or not by RFDSP.  0: No event is set by RFDSP  1: An event is set by RFDSP |
| 2 | RFTOA7IPCSTS<2> | R | 0 | RFDSP to A7 core IPC event 2 status.  Indicates to A7 whether the RFTOA7IPC event 2 is set or not by RFDSP.  0: No event is set by RFDSP  1: An event is set by RFDSP |
| 1 | RFTOA7IPCSTS<1> | R | 0 | RFDSP to A7 core IPC event 1 status.  Indicates to A7 whether the RFTOA7IPC event 1 is set or not by RFDSP.  0: No event is set by RFDSP  1: An event is set by RFDSP |
| 0 | RFTOA7IPCSTS<0> | R | 0 | RFDSP to A7 core IPC event 0 status.  Indicates to A7 whether the RFTOA7IPC event 0 is set or not by RFDSP.  0: No event is set by RFDSP  1: An event is set by RFDSP |

Note: IPC event status 0-7 will trigger interrupt to the A7 core via the GIC.

### A7TOPLCIPCSET<15:0>

A7 core to PLCDSP core IPC set register

Address Offset

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | A7TOPLCIPCSET<15> | W | 0 | A7 to PLCDSP core IPC flag 15 set.  Writing 1 to this bit sets the A7TOPLCIPCFLG<15> for the A7 and A7TOPLCIPCSTS<15> for the PLCDSP.  Writing 0 has no effect. |
| 14 | A7TOPLCIPCSET<14> | W | 0 | A7 to PLCDSP core IPC flag 14 set.  Writing 1 to this bit sets the A7TOPLCIPCFLG<14> for the A7 and A7TOPLCIPCSTS<14> for the PLCDSP.  Writing 0 has no effect. |
| 13 | A7TOPLCIPCSET<13> | W | 0 | A7 to PLCDSP core IPC flag 13 set.  Writing 1 to this bit sets the A7TOPLCIPCFLG<13> for the A7 and A7TOPLCIPCSTS<13> for the PLCDSP.  Writing 0 has no effect. |
| 12 | A7TOPLCIPCSET<12> | W | 0 | A7 to PLCDSP core IPC flag 12 set.  Writing 1 to this bit sets the A7TOPLCIPCFLG<12> for the A7 and A7TOPLCIPCSTS<12> for the PLCDSP.  Writing 0 has no effect. |
| 11 | A7TOPLCIPCSET<11> | W | 0 | A7 to PLCDSP core IPC flag 11 set.  Writing 1 to this bit sets the A7TOPLCIPCFLG<11> for the A7 and A7TOPLCIPCSTS<11> for the PLCDSP.  Writing 0 has no effect. |
| 10 | A7TOPLCIPCSET<10> | W | 0 | A7 to PLCDSP core IPC flag 10 set.  Writing 1 to this bit sets the A7TOPLCIPCFLG<10> for the A7 and A7TOPLCIPCSTS<10> for the PLCDSP.  Writing 0 has no effect. |
| 9 | A7TOPLCIPCSET<9 | W | 0 | A7 to PLCDSP core IPC flag 9 set.  Writing 1 to this bit sets the A7TOPLCIPCFLG<9> for the A7 and A7TOPLCIPCSTS<9> for the PLCDSP.  Writing 0 has no effect. |
| 8 | A7TOPLCIPCSET<8> | W | 0 | A7 to PLCDSP core IPC flag 8 set.  Writing 1 to this bit sets the A7TOPLCIPCFLG<8> for the A7 and A7TOPLCIPCSTS<8> for the PLCDSP.  Writing 0 has no effect. |
| 7 | A7TOPLCIPCSET<7> | W | 0 | A7 to PLCDSP core IPC flag 7 set.  Writing 1 to this bit sets the A7TOPLCIPCFLG<7> for the A7 and A7TOPLCIPCSTS<7> for the PLCDSP.  Writing 0 has no effect. |
| 6 | A7TOPLCIPCSET<6> | W | 0 | A7 to PLCDSP core IPC flag 6 set.  Writing 1 to this bit sets the A7TOPLCIPCFLG<6> for the A7 and A7TOPLCIPCSTS<6> for the PLCDSP.  Writing 0 has no effect. |
| 5 | A7TOPLCIPCSET<5> | W | 0 | A7 to PLCDSP core IPC flag 5 set.  Writing 1 to this bit sets the A7TOPLCIPCFLG<5> for the A7 and A7TOPLCIPCSTS<5> for the PLCDSP.  Writing 0 has no effect. |
| 4 | A7TOPLCIPCSET<4> | W | 0 | A7 to PLCDSP core IPC flag 4 set.  Writing 1 to this bit sets the A7TOPLCIPCFLG<4> for the A7 and A7TOPLCIPCSTS<4> for the PLCDSP.  Writing 0 has no effect. |
| 3 | A7TOPLCIPCSET<3> | W | 0 | A7 to PLCDSP core IPC flag 3 set.  Writing 1 to this bit sets the A7TOPLCIPCFLG<3> for the A7 and A7TOPLCIPCSTS<3> for the PLCDSP.  Writing 0 has no effect. |
| 2 | A7TOPLCIPCSET<2> | W | 0 | A7 to PLCDSP core IPC flag 2 set.  Writing 1 to this bit sets the A7TOPLCIPCFLG<2> for the A7 and A7TOPLCIPCSTS<2> for the PLCDSP.  Writing 0 has no effect. |
| 1 | A7TOPLCIPCSET<1> | W | 0 | A7 to PLCDSP core IPC flag 1 set.  Writing 1 to this bit sets the A7TOPLCIPCFLG<1> for the A7 and A7TOPLCIPCSTS<1> for the PLCDSP.  Writing 0 has no effect. |
| 0 | A7TOPLCIPCSET<0> | W | 0 | A7 to PLCDSP core IPC flag 0 set.  Writing 1 to this bit sets the A7TOPLCIPCFLG<0> for the A7 and A7TOPLCIPCSTS<0> for the PLCDSP.  Writing 0 has no effect. |

### A7TOPLCIPCCLR<15:0>

A7 core to PLCDSP core IPC clear register

Address Offset

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | A7TOPLCIPCCLR<15> | W | 0 | A7 to PLCDSP core IPC flag 15 clear.  Writing 1 to this bit clears the A7TOPLCIPCFLG<15> for the A7 and A7TOPLCIPCSTS<15> for the PLCDSP.  Writing 0 has no effect. |
| 14 | A7TOPLCIPCCLR<14> | W | 0 | A7 to PLCDSP core IPC flag 14 clear.  Writing 1 to this bit clears the A7TOPLCIPCFLG<14> for the A7 and A7TOPLCIPCSTS<14> for the PLCDSP.  Writing 0 has no effect. |
| 13 | A7TOPLCIPCCLR<13> | W | 0 | A7 to PLCDSP core IPC flag 13 clear.  Writing 1 to this bit clears the A7TOPLCIPCFLG<13> for the A7 and A7TOPLCIPCSTS<13> for the PLCDSP.  Writing 0 has no effect. |
| 12 | A7TOPLCIPCCLR<12> | W | 0 | A7 to PLCDSP core IPC flag 12 clear.  Writing 1 to this bit clears the A7TOPLCIPCFLG<12> for the A7 and A7TOPLCIPCSTS<12> for the PLCDSP.  Writing 0 has no effect. |
| 11 | A7TOPLCIPCCLR<11> | W | 0 | A7 to PLCDSP core IPC flag 11 clear.  Writing 1 to this bit clears the A7TOPLCIPCFLG<11> for the A7 and A7TOPLCIPCSTS<11> for the PLCDSP.  Writing 0 has no effect. |
| 10 | A7TOPLCIPCCLR<10> | W | 0 | A7 to PLCDSP core IPC flag 10 clear.  Writing 1 to this bit clears the A7TOPLCIPCFLG<10> for the A7 and A7TOPLCIPCSTS<10> for the PLCDSP.  Writing 0 has no effect. |
| 9 | A7TOPLCIPCCLR<9 | W | 0 | A7 to PLCDSP core IPC flag 9 clear.  Writing 1 to this bit clears the A7TOPLCIPCFLG<9> for the A7 and A7TOPLCIPCSTS<9> for the PLCDSP.  Writing 0 has no effect. |
| 8 | A7TOPLCIPCCLR<8> | W | 0 | A7 to PLCDSP core IPC flag 8 clear.  Writing 1 to this bit clears the A7TOPLCIPCFLG<8> for the A7 and A7TOPLCIPCSTS<8> for the PLCDSP.  Writing 0 has no effect. |
| 7 | A7TOPLCIPCCLR<7> | W | 0 | A7 to PLCDSP core IPC flag 7 clear.  Writing 1 to this bit clears the A7TOPLCIPCFLG<7> for the A7 and A7TOPLCIPCSTS<7> for the PLCDSP.  Writing 0 has no effect. |
| 6 | A7TOPLCIPCCLR<6> | W | 0 | A7 to PLCDSP core IPC flag 6 clear.  Writing 1 to this bit clears the A7TOPLCIPCFLG<6> for the A7 and A7TOPLCIPCSTS<6> for the PLCDSP.  Writing 0 has no effect. |
| 5 | A7TOPLCIPCCLR<5> | W | 0 | A7 to PLCDSP core IPC flag 5 clear.  Writing 1 to this bit clears the A7TOPLCIPCFLG<5> for the A7 and A7TOPLCIPCSTS<5> for the PLCDSP.  Writing 0 has no effect. |
| 4 | A7TOPLCIPCCLR<4> | W | 0 | A7 to PLCDSP core IPC flag 4 clear.  Writing 1 to this bit clears the A7TOPLCIPCFLG<4> for the A7 and A7TOPLCIPCSTS<4> for the PLCDSP.  Writing 0 has no effect. |
| 3 | A7TOPLCIPCCLR<3> | W | 0 | A7 to PLCDSP core IPC flag 3 clear.  Writing 1 to this bit clears the A7TOPLCIPCFLG<3> for the A7 and A7TOPLCIPCSTS<3> for the PLCDSP.  Writing 0 has no effect. |
| 2 | A7TOPLCIPCCLR<2> | W | 0 | A7 to PLCDSP core IPC flag 2 clear.  Writing 1 to this bit clears the A7TOPLCIPCFLG<2> for the A7 and A7TOPLCIPCSTS<2> for the PLCDSP.  Writing 0 has no effect. |
| 1 | A7TOPLCIPCCLR<1> | W | 0 | A7 to PLCDSP core IPC flag 1 clear.  Writing 1 to this bit clears the A7TOPLCIPCFLG<1> for the A7 and A7TOPLCIPCSTS<1> for the PLCDSP.  Writing 0 has no effect. |
| 0 | A7TOPLCIPCCLR<0> | W | 0 | A7 to PLCDSP core IPC flag 0 clear.  Writing 1 to this bit clears the A7TOPLCIPCFLG<0> for the A7 and A7TOPLCIPCSTS<0> for the PLCDSP.  Writing 0 has no effect. |

Notes: Normally, PLCDSP will clear (acknowledge) the A7toPLC IPC event flags. This mechanism may be useful if PLCDSP is non-responsive.

### A7TOPLCIPCFLG<15:0>

A7 core to PLCDSP core IPC flags register

Address Offset

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | A7TOPLCIPCFLG<15> | R | 0 | A7 to PLCDSP core IPC flag 15 status.  Indicates to A7 whether theA7TOPLC IPCFLG<15> is set.  0: The event flag is not set  1: The event flag is set |
| 14 | A7TOPLCIPCFLG<14> | R | 0 | A7 to PLCDSP core IPC flag 14 status.  Indicates to A7 whether theA7TOPLC IPCFLG<14> is set.  0: The event flag is not set  1: The event flag is set |
| 13 | A7TOPLCIPCFLG<13> | R | 0 | A7 to PLCDSP core IPC flag 13 status.  Indicates to A7 whether theA7TOPLC IPCFLG<13> is set.  0: The event flag is not set  1: The event flag is set |
| 12 | A7TOPLCIPCFLG<12> | R | 0 | A7 to PLCDSP core IPC flag 12 status.  Indicates to A7 whether theA7TOPLC IPCFLG<12> is set.  0: The event flag is not set  1: The event flag is set |
| 11 | A7TOPLCIPCFLG<11> | R | 0 | A7 to PLCDSP core IPC flag 11 status.  Indicates to A7 whether theA7TOPLC IPCFLG<11> is set.  0: The event flag is not set  1: The event flag is set |
| 10 | A7TOPLCIPCFLG<10> | R | 0 | A7 to PLCDSP core IPC flag 10 status.  Indicates to A7 whether theA7TOPLC IPCFLG<10> is set.  0: The event flag is not set  1: The event flag is set |
| 9 | A7TOPLCIPCFLG<9 | R | 0 | A7 to PLCDSP core IPC flag 9 status.  Indicates to A7 whether theA7TOPLC IPCFLG<9> is set.  0: The event flag is not set  1: The event flag is set |
| 8 | A7TOPLCIPCFLG<8> | R | 0 | A7 to PLCDSP core IPC flag 8 status.  Indicates to A7 whether theA7TOPLC IPCFLG<8> is set.  0: The event flag is not set  1: The event flag is set |
| 7 | A7TOPLCIPCFLG<7> | R | 0 | A7 to PLCDSP core IPC flag 7 status.  Indicates to A7 whether theA7TOPLC IPCFLG<7> is set.  0: The event flag is not set  1: The event flag is set |
| 6 | A7TOPLCIPCFLG<6> | R | 0 | A7 to PLCDSP core IPC flag 6 status.  Indicates to A7 whether theA7TOPLC IPCFLG<6> is set.  0: The event flag is not set  1: The event flag is set |
| 5 | A7TOPLCIPCFLG<5> | R | 0 | A7 to PLCDSP core IPC flag 5 status.  Indicates to A7 whether theA7TOPLC IPCFLG<5> is set.  0: The event flag is not set  1: The event flag is set |
| 4 | A7TOPLCIPCFLG<4> | R | 0 | A7 to PLCDSP core IPC flag 4 status.  Indicates to A7 whether theA7TOPLC IPCFLG<4> is set.  0: The event flag is not set  1: The event flag is set |
| 3 | A7TOPLCIPCFLG<3> | R | 0 | A7 to PLCDSP core IPC flag 3 status.  Indicates to A7 whether theA7TOPLC IPCFLG<3> is set.  0: The event flag is not set  1: The event flag is set |
| 2 | A7TOPLCIPCFLG<2> | R | 0 | A7 to PLCDSP core IPC flag 2 status.  Indicates to A7 whether theA7TOPLC IPCFLG<2> is set.  0: The event flag is not set  1: The event flag is set |
| 1 | A7TOPLCIPCFLG<1> | R | 0 | A7 to PLCDSP core IPC flag 1 status.  Indicates to A7 whether theA7TOPLC IPCFLG<1> is set.  0: The event flag is not set  1: The event flag is set |
| 0 | A7TOPLCIPCFLG<0> | R | 0 | A7 to PLCDSP core IPC flag 0 status.  Indicates to A7 whether theA7TOPLC IPCFLG<0> is set.  0: The event flag is not set  1: The event flag is set |

### PLCTOA7IPCACK<15:0>

PLCDSP core to A7 core IPC event acknowledge register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | PLCTOA7IPCACK<15> | W | 0 | PLCDSP to A7 IPC event 15 acknowledge.  Writing 1 to this bit clears the PLCTOA7IPCFLG<15> and PLCTOA7IPCSTS<15> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 14 | PLCTOA7IPCACK<14> | W | 0 | PLCDSP to A7 IPC event 14 acknowledge.  Writing 1 to this bit clears the PLCTOA7IPCFLG<14> and PLCTOA7IPCSTS<14> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 13 | PLCTOA7IPCACK<13> | W | 0 | PLCDSP to A7 IPC event 13 acknowledge.  Writing 1 to this bit clears the PLCTOA7IPCFLG<13> and PLCTOA7IPCSTS<13> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 12 | PLCTOA7IPCACK<12> | W | 0 | PLCDSP to A7 IPC event 12 acknowledge.  Writing 1 to this bit clears the PLCTOA7IPCFLG<12> and PLCTOA7IPCSTS<12> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 11 | PLCTOA7IPCACK<11> | W | 0 | PLCDSP to A7 IPC event 11 acknowledge.  Writing 1 to this bit clears the PLCTOA7IPCFLG<11> and PLCTOA7IPCSTS<11> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 10 | PLCTOA7IPCACK<10> | W | 0 | PLCDSP to A7 IPC event 10 acknowledge.  Writing 1 to this bit clears the PLCTOA7IPCFLG<10> and PLCTOA7IPCSTS<10> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 9 | PLCTOA7IPCACK<9 | W | 0 | PLCDSP to A7 IPC event 9 acknowledge.  Writing 1 to this bit clears the PLCTOA7IPCFLG<9> and PLCTOA7IPCSTS<9> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 8 | PLCTOA7IPCACK<8> | W | 0 | PLCDSP to A7 IPC event 8 acknowledge.  Writing 1 to this bit clears the PLCTOA7IPCFLG<8> and PLCTOA7IPCSTS<8> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 7 | PLCTOA7IPCACK<7> | W | 0 | PLCDSP to A7 IPC event 7 acknowledge.  Writing 1 to this bit clears the PLCTOA7IPCFLG<7> and PLCTOA7IPCSTS<7> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 6 | PLCTOA7IPCACK<6> | W | 0 | PLCDSP to A7 IPC event 6 acknowledge.  Writing 1 to this bit clears the PLCTOA7IPCFLG<6> and PLCTOA7IPCSTS<6> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 5 | PLCTOA7IPCACK<5> | W | 0 | PLCDSP to A7 IPC event 5 acknowledge.  Writing 1 to this bit clears the PLCTOA7IPCFLG<5> and PLCTOA7IPCSTS<5> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 4 | PLCTOA7IPCACK<4> | W | 0 | PLCDSP to A7 IPC event 4 acknowledge.  Writing 1 to this bit clears the PLCTOA7IPCFLG<4> and PLCTOA7IPCSTS<4> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 3 | PLCTOA7IPCACK<3> | W | 0 | PLCDSP to A7 IPC event 3 acknowledge.  Writing 1 to this bit clears the PLCTOA7IPCFLG<3> and PLCTOA7IPCSTS<3> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 2 | PLCTOA7IPCACK<2> | W | 0 | PLCDSP to A7 IPC event 2 acknowledge.  Writing 1 to this bit clears the PLCTOA7IPCFLG<2> and PLCTOA7IPCSTS<2> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 1 | PLCTOA7IPCACK<1> | W | 0 | PLCDSP to A7 IPC event 1 acknowledge.  Writing 1 to this bit clears the PLCTOA7IPCFLG<1> and PLCTOA7IPCSTS<1> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 0 | PLCTOA7IPCACK<0> | W | 0 | PLCDSP to A7 IPC event 0 acknowledge.  Writing 1 to this bit clears the PLCTOA7IPCFLG<0> and PLCTOA7IPCSTS<0> which are set by PLCDSP.  Writing 0 to this bit has no effect |

### PLCTOA7IPCSTS<15:0>

PLCDSP core to A7 core IPC event status register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | PLCTOA7IPCSTS<15> | R | 0 | PLCDSP to A7 core IPC event 15 status.  Indicates to A7 whether the PLCTOA7IPC event 15 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 14 | PLCTOA7IPCSTS<14> | R | 0 | PLCDSP to A7 core IPC event 14 status.  Indicates to A7 whether the PLCTOA7IPC event 14 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 13 | PLCTOA7IPCSTS<13> | R | 0 | PLCDSP to A7 core IPC event 13 status.  Indicates to A7 whether the PLCTOA7IPC event 13 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 12 | PLCTOA7IPCSTS<12> | R | 0 | PLCDSP to A7 core IPC event 12 status.  Indicates to A7 whether the PLCTOA7IPC event 12 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 11 | PLCTOA7IPCSTS<11> | R | 0 | PLCDSP to A7 core IPC event 11 status.  Indicates to A7 whether the PLCTOA7IPC event 11 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 10 | PLCTOA7IPCSTS<10> | R | 0 | PLCDSP to A7 core IPC event 10 status.  Indicates to A7 whether the PLCTOA7IPC event 10 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 9 | PLCTOA7IPCSTS<9 | R | 0 | PLCDSP to A7 core IPC event 9 status.  Indicates to A7 whether the PLCTOA7IPC event 9 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 8 | PLCTOA7IPCSTS<8> | R | 0 | PLCDSP to A7 core IPC event 8 status.  Indicates to A7 whether the PLCTOA7IPC event 8 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 7 | PLCTOA7IPCSTS<7> | R | 0 | PLCDSP to A7 core IPC event 7 status.  Indicates to A7 whether the PLCTOA7IPC event 7 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 6 | PLCTOA7IPCSTS<6> | R | 0 | PLCDSP to A7 core IPC event 6 status.  Indicates to A7 whether the PLCTOA7IPC event 6 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 5 | PLCTOA7IPCSTS<5> | R | 0 | PLCDSP to A7 core IPC event 5 status.  Indicates to A7 whether the PLCTOA7IPC event 5 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 4 | PLCTOA7IPCSTS<4> | R | 0 | PLCDSP to A7 core IPC event 4 status.  Indicates to A7 whether the PLCTOA7IPC event 4 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 3 | PLCTOA7IPCSTS<3> | R | 0 | PLCDSP to A7 core IPC event 3 status.  Indicates to A7 whether the PLCTOA7IPC event 3 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 2 | PLCTOA7IPCSTS<2> | R | 0 | PLCDSP to A7 core IPC event 2 status.  Indicates to A7 whether the PLCTOA7IPC event 2 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 1 | PLCTOA7IPCSTS<1> | R | 0 | PLCDSP to A7 core IPC event 1 status.  Indicates to A7 whether the PLCTOA7IPC event 1 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 0 | PLCTOA7IPCSTS<0> | R | 0 | PLCDSP to A7 core IPC event 0 status.  Indicates to A7 whether the PLCTOA7IPC event 0 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |

Note: IPC event status 0-7 will trigger interrupt to the A7 core via the GIC.

### RFTOA7IPCTEST<31:0>

RF To A7 Interrupt test register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:8 | reserved |  |  | Reserved |
| 7:0 | RFTOA7IPCTEST | R/W | 0 | To force IPC\_RFTOA7\_INT to be triggered, it is for debugging purpose only.  When write 1 to any bit of RFTOA7IPCTEST, corresponding bit on IPC\_RFTOA7\_INT[7:0] is asserted  When write 0, RFTOA7IPCTEST has no effect on IPC\_RFTOA7\_INT[7:0] |

### PLCTOA7IPCTEST<31:0>

PLC To A7 Interrupt test register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:8 | reserved |  |  | Reserved |
| 7:0 | PLCTOA7IPCTEST | R/W | 0 | To force IPC\_PLCTOA7\_INT to be triggered, it is for debugging purpose only.  When write 1 to any bit of PLCTOA7IPCTEST, corresponding bit on IPC\_PLCTOA7\_INT[7:0] is asserted  When write 0, PLCTOA7IPCTEST has no effect on IPC\_PLCTOA7\_INT[7:0] |

### PLCTOA7ACK\_INT\_CLR<31:0>

PLC to A7 ACK interrupt clear register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:8 | reserved |  |  | Reserved |
| 7:0 | PLCTOA7ACK\_INT\_CLR[7:0] | W | 0 | To clear PLC to A7 ACK interrupt flag  When write 1, PLCTOA7\_ACK\_INT is cleared |

### RFTOA7ACK\_INT\_CLR<31:0>

RF to A7 ACK interrupt clear register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:8 | reserved |  |  | Reserved |
| 7:0 | RFTOA7ACK\_INT\_CLR[7:0] | W | 0 | To clear RF to A7 ACK interrupt flag  When write 1, RFTOA7\_ACK\_INT is cleared |

### A7SRP00REQ<31:0>

Shared RAM page0 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 0 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP01REQ<31:0>

Shared RAM page1 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 1 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP02REQ<31:0>

Shared RAM page2 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 2 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP03REQ<31:0>

Shared RAM page3 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 3 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP04REQ<31:0>

Shared RAM page4 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page4 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP05REQ<31:0>

Shared RAM page5 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 5 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP06REQ<31:0>

Shared RAM page6 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 6 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP07REQ<31:0>

Shared RAM page7 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page7 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP08REQ<31:0>

Shared RAM page8 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 8 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP09REQ<31:0>

Shared RAM page9 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 9 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP10REQ<31:0>

Shared RAM page10 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page1 0 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP11REQ<31:0>

Shared RAM page11 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 11 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP12REQ<31:0>

Shared RAM page12 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 12 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP13REQ<31:0>

Shared RAM page13 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 13 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP14REQ<31:0>

Shared RAM page14 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 14 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP15REQ<31:0>

Shared RAM page15 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page15 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP16REQ<31:0>

Shared RAM page16 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 16 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP17REQ<31:0>

Shared RAM page17 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page17 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP18REQ<31:0>

Shared RAM page18 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 18 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP19REQ<31:0>

Shared RAM page19 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 19 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP20REQ<31:0>

Shared RAM page20 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 20 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP21REQ<31:0>

Shared RAM page21 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 21 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP22REQ<31:0>

Shared RAM page22 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 22 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP23REQ<31:0>

Shared RAM page23 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 23 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP24REQ<31:0>

Shared RAM page24 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 24 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP25REQ<31:0>

Shared RAM page25 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 25 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP26REQ<31:0>

Shared RAM page26 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 26 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP27REQ<31:0>

Shared RAM page27 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 27 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP28REQ<31:0>

Shared RAM page28 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 28 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP29REQ<31:0>

Shared RAM page29 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 29 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP30REQ<31:0>

Shared RAM page30 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 30 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### A7SRP31REQ<31:0>

Shared RAM page31 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0xBE97A3D will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 31 write access request semaphore from A7:  Write a value “01” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RF DSP core IPC registers

### A7TORFIPCCOMM<31:0>

A7 core to RFDSP core IPC command register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | COMMAND | R | 0 | This is a general purpose register used to send software-defined commands from A7 to RFDSP. |

### A7TORFIPCADDR<31:0>

A7 core to RFDSP core IPC address register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | ADDRESS | R | 0 | This is a general purpose register used to send software-defined address from A7 to RFDSP. |

### A7TORFIPCDATA0<31:0>

A7 core to RFDSP core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA0 | R | 0 | This is a general purpose register used to send software-defined data from A7 to RFDSP. |

### A7TORFIPCDATA1<31:0>

A7 core to RFDSP core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA1 | R- | 0 | This is a general purpose register used to used to send software-defined data from A7 to RFDSP. |

### RFTOA7IPCCOMM<31:0>

RFDSP core to A7 core IPC command register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | COMMAND | R/W | 0 | This is a general purpose register used to send software-defined commands from RFDSP to A7. |

### RFTOA7IPCADDR<31:0>

RFDSP core to A7 core IPC address register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | ADDRESS | R/W | 0 | This is a general purpose register used to send software-defined address from RFDSP to A7. |

### RFTOA7IPCDATA0<31:0>

RFDSP core to A7 core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA0 | R/W | 0 | This is a general purpose register used to send software-defined data from RFDSP to A7. |

### RFTOA7IPCDATA1<31:0>

RFDSP core to A7 core IPC response register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA1 | R/W | 0 | This is a general purpose register used to to send software-defined data from RFDSP to A7. |

### RFTOPLCIPCCOMM<31:0>

RFDSP core to PLCDSP core IPC command register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | COMMAND | R/W | 0 | This is a general purpose register used to send software-defined commands from RFDSP to PLCDSP. |

### RFTOPLCIPCADDR<31:0>

RFDSP core to PLCDSP core IPC address register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | ADDRESS | R/W | 0 | This is a general purpose register used to send software-defined address from RFDSP to PLCDSP. |

### RFTOPLCIPCDATA0<31:0>

RFDSP core to PLCDSP core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA0 | R/W | 0 | This is a general purpose register used to send software-defined data from RFDSP to PLCDSP. |

### RFTOPLCIPCDATA1<31:0>

RFDSP core to PLCDSP core IPC response register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA1 | R/W | 0 | This is a general purpose register used to send software-defined data from RFDSP to PLCDSP. |

### PLCTORFIPCCOMM<31:0>

PLCDSP core to RFDSP core IPC command register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | COMMAND | R | 0 | This is a general purpose register used to send software-defined commands from PLCDSP to RFDSP. |

### PLCTORFIPCADDR<31:0>

PLCDSP core to RFDSP core IPC address register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | ADDRESS | R | 0 | This is a general purpose register used to send software-defined address from PLCDSP to RFDSP. |

### PLCTORFIPCDATA0<31:0>

PLCDSP core to RFDSP core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA0 | R | 0 | This is a general purpose register used to send software-defined data from PLCDSP to RFDSP. |

### PLCTORFIPCDATA1<31:0>

PLCDSP core to RFDSP core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA1 | R- | 0 | This is a general purpose register used to to send software-defined data from PLCDSP to RFDSP. |

### IPCTMRSCALER <31:0>

Free running 64bit timestamp counter prescaler register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15:0 | PRESCALER | R/W | 0 | The prescaler value used to derive the free running timer’s clock: Ftimer=Fcpu/(prescaler+1).  Prescale counter is reset whenever this setting or IPCTMRCNT is changed  It can be only configured by RF Core |

### IPCCOUNTERL <31:0>

Free running 64bit timestamp counter low register.

To ensure the integrity of read data from AHB bus, a snapshot for the high 32-bits counter is taken when a read is performed on the IPCCOUNTERL register. When the RF DSP core reads the IPCOUNTERH, the snapshot is fed back to the user instead of the current value in the IPCOUNTERH register. Therefore, the user application software must always read IPCCOUNTERL first and then read IPCCOUNTERH.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | IPCCOUNTERL | R | 0 | This is the lower 32-bits of free running 64 bit timestamp counter clocked by the divided clock. |

### IPCCOUNTERH <31:0>

Free running 64bit timestamp counter high register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | IPCCOUNTERH | R | 0 | This is the upper 32-bits of free running 64 bit timestamp counter clocked by the divided clock. |

### IPCTMRCONT <31:0>

Free running 64bit control register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:1 | Reserved |  |  |  |
| 0 | TMRCOUNTUP | R/W | 1 | 0x1: Timer as upward counter  0x0: Timer as downward counter  It can be only configured by RF Core  Timer count value is reset to 0x0 (count up) or 0xffffffff\_ffffffff (count down) whenever TMRCOUNTUP setting is changed |

### SRMSEL0<31:0>

Shared RAM pages’ ownership (master selection) status register0

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:30 | SRP15OWN | R | 0 | Shared RAM page15 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 29:28 | SRP14OWN | R | 0 | Shared RAM page 14 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 27:26 | SRP13OWN | R | 0 | Shared RAM page 13 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 25:24 | SRP12OWN | R | 0 | Shared RAM page 12 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 23:22 | SRP110OWN | R | 0 | Shared RAM page 11 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 21:20 | SRP10OWN | R | 0 | Shared RAM page 10 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 19:18 | SRP09OWN | R | 0 | Shared RAM page 9 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 17:16 | SRP08OWN | R | 0 | Shared RAM page 8 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 15:14 | SRP07OWN | R | 0 | Shared RAM page 7 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 13:12 | SRP06OWN | R | 0 | Shared RAM page 6 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 11:10 | SRP05OWN | R | 0 | Shared RAM page 5 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 9:8 | SRP04OWN | R | 0 | Shared RAM page 4 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 7:6 | SRP03OWN | R | 0 | Shared RAM page 3 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 5:4 | SRP02OWN | R | 0 | Shared RAM page 2 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 3:2 | SRP01OWN | R | 0 | Shared RAM page 1 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 1:0 | SRP00OWN | R | 0 | Shared RAM page 0 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |

### SRMSEL1<31:0>

Shared RAM pages’ ownership (master selection) status register1

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:30 | SRP31OWN | R | 0 | Shared RAM page 31 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 29:28 | SRP30OWN | R | 0 | Shared RAM page 30 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 27:26 | SRP29OWN | R | 0 | Shared RAM page 29 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 25:24 | SRP28OWN | R | 0 | Shared RAM page 28 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 23:22 | SRP270OWN | R | 0 | Shared RAM page 27 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 21:20 | SRP26OWN | R | 0 | Shared RAM page 26 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 19:18 | SRP25OWN | R | 0 | Shared RAM page 25 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 17:16 | SRP24OWN | R | 0 | Shared RAM page 24 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 15:14 | SRP23OWN | R | 0 | Shared RAM page 23 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 13:12 | SRP22OWN | R | 0 | Shared RAM page 22 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 11:10 | SRP21OWN | R | 0 | Shared RAM page 21 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 9:8 | SRP20OWN | R | 0 | Shared RAM page 20 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 7:6 | SRP19OWN | R | 0 | Shared RAM page 19 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 5:4 | SRP18OWN | R | 0 | Shared RAM page 18 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 3:2 | SRP17OWN | R | 0 | Shared RAM page 17 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 1:0 | SRP16OWN | R | 0 | Shared RAM page 16 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |

### RFTOA7IPCSET<15:0>

RFDSP core to A7 core IPC set register

Address Offset

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | RFTOA7IPCSET<15> | W | 0 | RFDSP to A7 core IPC flag 15 set.  Writing 1 to this bit sets the RFTOA7IPCFLG<15> for the RFDSP and RFTOA7IPCSTS<15> for the A7.  Writing 0 has no effect. |
| 14 | RFTOA7IPCSET<14> | W | 0 | RFDSP to A7 core IPC flag 14 set.  Writing 1 to this bit sets the RFTOA7IPCFLG<14> for the RFDSP and RFTOA7IPCSTS<14> for the A7.  Writing 0 has no effect. |
| 13 | RFTOA7IPCSET<13> | W | 0 | RFDSP to A7 core IPC flag 13 set.  Writing 1 to this bit sets the RFTOA7IPCFLG<13> for the RFDSP and RFTOA7IPCSTS<13> for the A7.  Writing 0 has no effect. |
| 12 | RFTOA7IPCSET<12> | W | 0 | RFDSP to A7 core IPC flag 12 set.  Writing 1 to this bit sets the RFTOA7IPCFLG<12> for the RFDSP and RFTOA7IPCSTS<12> for the A7.  Writing 0 has no effect. |
| 11 | RFTOA7IPCSET<11> | W | 0 | RFDSP to A7 core IPC flag 11 set.  Writing 1 to this bit sets the RFTOA7IPCFLG<11> for the RFDSP and RFTOA7IPCSTS<11> for the A7.  Writing 0 has no effect. |
| 10 | RFTOA7IPCSET<10> | W | 0 | RFDSP to A7 core IPC flag 10 set.  Writing 1 to this bit sets the RFTOA7IPCFLG<10> for the RFDSP and RFTOA7IPCSTS<10> for the A7.  Writing 0 has no effect. |
| 9 | RFTOA7IPCSET<9 | W | 0 | RFDSP to A7 core IPC flag 9 set.  Writing 1 to this bit sets the RFTOA7IPCFLG<9> for the RFDSP and RFTOA7IPCSTS<9> for the A7.  Writing 0 has no effect. |
| 8 | RFTOA7IPCSET<8> | W | 0 | RFDSP to A7 core IPC flag 8 set.  Writing 1 to this bit sets the RFTOA7IPCFLG<8> for the RFDSP and RFTOA7IPCSTS<8> for the A7.  Writing 0 has no effect. |
| 7 | RFTOA7IPCSET<7> | W | 0 | RFDSP to A7 core IPC flag 7 set.  Writing 1 to this bit sets the RFTOA7IPCFLG<7> for the RFDSP and RFTOA7IPCSTS<7> for the A7.  Writing 0 has no effect. |
| 6 | RFTOA7IPCSET<6> | W | 0 | RFDSP to A7 core IPC flag 6 set.  Writing 1 to this bit sets the RFTOA7IPCFLG<6> for the RFDSP and RFTOA7IPCSTS<6> for the A7.  Writing 0 has no effect. |
| 5 | RFTOA7IPCSET<5> | W | 0 | RFDSP to A7 core IPC flag 5 set.  Writing 1 to this bit sets the RFTOA7IPCFLG<5> for the RFDSP and RFTOA7IPCSTS<5> for the A7.  Writing 0 has no effect. |
| 4 | RFTOA7IPCSET<4> | W | 0 | RFDSP to A7 core IPC flag 4 set.  Writing 1 to this bit sets the RFTOA7IPCFLG<4> for the RFDSP and RFTOA7IPCSTS<4> for the A7.  Writing 0 has no effect. |
| 3 | RFTOA7IPCSET<3> | W | 0 | RFDSP to A7 core IPC flag 3 set.  Writing 1 to this bit sets the RFTOA7IPCFLG<3> for the RFDSP and RFTOA7IPCSTS<3> for the A7.  Writing 0 has no effect. |
| 2 | RFTOA7IPCSET<2> | W | 0 | RFDSP to A7 core IPC flag 2 set.  Writing 1 to this bit sets the RFTOA7IPCFLG<2> for the RFDSP and RFTOA7IPCSTS<2> for the A7.  Writing 0 has no effect. |
| 1 | RFTOA7IPCSET<1> | W | 0 | RFDSP to A7 core IPC flag 1 set.  Writing 1 to this bit sets the RFTOA7IPCFLG<1> for the RFDSP and RFTOA7IPCSTS<1> for the A7.  Writing 0 has no effect. |
| 0 | RFTOA7IPCSET<0> | W | 0 | RFDSP to A7 core IPC flag 0 set.  Writing 1 to this bit sets the RFTOA7IPCFLG<0> for the RFDSP and RFTOA7IPCSTS<0> for the A7.  Writing 0 has no effect. |

### RFTOA7IPCCLR<15:0>

RFDSP core to A7 core IPC clear register

Address Offset

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | RFTOA7IPCCLR<15> | W | 0 | RFDSP to A7 core IPC flag 15 clear.  Writing 1 to this bit clears the RFTOA7IPCFLG<15> for the RFDSP and RFTOA7IPCSTS<15> for the A7.  Writing 0 has no effect. |
| 14 | RFTOA7IPCCLR<14> | W | 0 | RFDSP to A7 core IPC flag 14 clear.  Writing 1 to this bit clears the RFTOA7IPCFLG<14> for the RFDSP and RFTOA7IPCSTS<14> for the A7.  Writing 0 has no effect. |
| 13 | RFTOA7IPCCLR<13> | W | 0 | RFDSP to A7 core IPC flag 13 clear.  Writing 1 to this bit clears the RFTOA7IPCFLG<13> for the RFDSP and RFTOA7IPCSTS<13> for the A7.  Writing 0 has no effect. |
| 12 | RFTOA7IPCCLR<12> | W | 0 | RFDSP to A7 core IPC flag 12 clear.  Writing 1 to this bit clears the RFTOA7IPCFLG<12> for the RFDSP and RFTOA7IPCSTS<12> for the A7.  Writing 0 has no effect. |
| 11 | RFTOA7IPCCLR<11> | W | 0 | RFDSP to A7 core IPC flag 11 clear.  Writing 1 to this bit clears the RFTOA7IPCFLG<11> for the RFDSP and RFTOA7IPCSTS<11> for the A7.  Writing 0 has no effect. |
| 10 | RFTOA7IPCCLR<10> | W | 0 | RFDSP to A7 core IPC flag 10 clear.  Writing 1 to this bit clears the RFTOA7IPCFLG<10> for the RFDSP and RFTOA7IPCSTS<10> for the A7.  Writing 0 has no effect. |
| 9 | RFTOA7IPCCLR<9 | W | 0 | RFDSP to A7 core IPC flag 9 clear.  Writing 1 to this bit clears the RFTOA7IPCFLG<9> for the RFDSP and RFTOA7IPCSTS<9> for the A7.  Writing 0 has no effect. |
| 8 | RFTOA7IPCCLR<8> | W | 0 | RFDSP to A7 core IPC flag 8 clear.  Writing 1 to this bit clears the RFTOA7IPCFLG<8> for the RFDSP and RFTOA7IPCSTS<8> for the A7.  Writing 0 has no effect. |
| 7 | RFTOA7IPCCLR<7> | W | 0 | RFDSP to A7 core IPC flag 7 clear.  Writing 1 to this bit clears the RFTOA7IPCFLG<7> for the RFDSP and RFTOA7IPCSTS<7> for the A7.  Writing 0 has no effect. |
| 6 | RFTOA7IPCCLR<6> | W | 0 | RFDSP to A7 core IPC flag 6 clear.  Writing 1 to this bit clears the RFTOA7IPCFLG<6> for the RFDSP and RFTOA7IPCSTS<6> for the A7.  Writing 0 has no effect. |
| 5 | RFTOA7IPCCLR<5> | W | 0 | RFDSP to A7 core IPC flag 5 clear.  Writing 1 to this bit clears the RFTOA7IPCFLG<5> for the RFDSP and RFTOA7IPCSTS<5> for the A7.  Writing 0 has no effect. |
| 4 | RFTOA7IPCCLR<4> | W | 0 | RFDSP to A7 core IPC flag 4 clear.  Writing 1 to this bit clears the RFTOA7IPCFLG<4> for the RFDSP and RFTOA7IPCSTS<4> for the A7.  Writing 0 has no effect. |
| 3 | RFTOA7IPCCLR<3> | W | 0 | RFDSP to A7 core IPC flag 3 clear.  Writing 1 to this bit clears the RFTOA7IPCFLG<3> for the RFDSP and RFTOA7IPCSTS<3> for the A7.  Writing 0 has no effect. |
| 2 | RFTOA7IPCCLR<2> | W | 0 | RFDSP to A7 core IPC flag 2 clear.  Writing 1 to this bit clears the RFTOA7IPCFLG<2> for the RFDSP and RFTOA7IPCSTS<2> for the A7.  Writing 0 has no effect. |
| 1 | RFTOA7IPCCLR<1> | W | 0 | RFDSP to A7 core IPC flag 1 clear.  Writing 1 to this bit clears the RFTOA7IPCFLG<1> for the RFDSP and RFTOA7IPCSTS<1> for the A7.  Writing 0 has no effect. |
| 0 | RFTOA7IPCCLR<0> | W | 0 | RFDSP to A7 core IPC flag 0 clear.  Writing 1 to this bit clears the RFTOA7IPCFLG<0> for the RFDSP and RFTOA7IPCSTS<0> for the A7.  Writing 0 has no effect. |

Notes: Normally, A7 will clear (acknowledge) the RFtoA7 IPC event flags. This mechanism may be useful if A7 is non-responsive.

### RFTOA7IPCFLG<15:0>

RFDSP core to A7 core IPC flags register

Address Offset

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | RFTOA7IPCFLG<15> | R | 0 | RFDSP to A7 core IPC flag 15 status.  Indicates to RFDSP whether theRFTOA7 IPCFLG<15> is set.  0: The event flag is not set  1: The event flag is set |
| 14 | RFTOA7IPCFLG<14> | R | 0 | RFDSP to A7 core IPC flag 14 status.  Indicates to RFDSP whether theRFTOA7 IPCFLG<14> is set.  0: The event flag is not set  1: The event flag is set |
| 13 | RFTOA7IPCFLG<13> | R | 0 | RFDSP to A7 core IPC flag 13 status.  Indicates to RFDSP whether theRFTOA7 IPCFLG<13> is set.  0: The event flag is not set  1: The event flag is set |
| 12 | RFTOA7IPCFLG<12> | R | 0 | RFDSP to A7 core IPC flag 12 status.  Indicates to RFDSP whether theRFTOA7 IPCFLG<12> is set.  0: The event flag is not set  1: The event flag is set |
| 11 | RFTOA7IPCFLG<11> | R | 0 | RFDSP to A7 core IPC flag 11 status.  Indicates to RFDSP whether theRFTOA7 IPCFLG<11> is set.  0: The event flag is not set  1: The event flag is set |
| 10 | RFTOA7IPCFLG<10> | R | 0 | RFDSP to A7 core IPC flag 10 status.  Indicates to RFDSP whether theRFTOA7 IPCFLG<10> is set.  0: The event flag is not set  1: The event flag is set |
| 9 | RFTOA7IPCFLG<9 | R | 0 | RFDSP to A7 core IPC flag 9 status.  Indicates to RFDSP whether theRFTOA7 IPCFLG<9> is set.  0: The event flag is not set  1: The event flag is set |
| 8 | RFTOA7IPCFLG<8> | R | 0 | RFDSP to A7 core IPC flag 8 status.  Indicates to RFDSP whether theRFTOA7 IPCFLG<8> is set.  0: The event flag is not set  1: The event flag is set |
| 7 | RFTOA7IPCFLG<7> | R | 0 | RFDSP to A7 core IPC flag 7 status.  Indicates to RFDSP whether theRFTOA7 IPCFLG<7> is set.  0: The event flag is not set  1: The event flag is set |
| 6 | RFTOA7IPCFLG<6> | R | 0 | RFDSP to A7 core IPC flag 6 status.  Indicates to RFDSP whether theRFTOA7 IPCFLG<6> is set.  0: The event flag is not set  1: The event flag is set |
| 5 | RFTOA7IPCFLG<5> | R | 0 | RFDSP to A7 core IPC flag 5 status.  Indicates to RFDSP whether theRFTOA7 IPCFLG<5> is set.  0: The event flag is not set  1: The event flag is set |
| 4 | RFTOA7IPCFLG<4> | R | 0 | RFDSP to A7 core IPC flag 4 status.  Indicates to RFDSP whether theRFTOA7 IPCFLG<4> is set.  0: The event flag is not set  1: The event flag is set |
| 3 | RFTOA7IPCFLG<3> | R | 0 | RFDSP to A7 core IPC flag 3 status.  Indicates to RFDSP whether theRFTOA7 IPCFLG<3> is set.  0: The event flag is not set  1: The event flag is set |
| 2 | RFTOA7IPCFLG<2> | R | 0 | RFDSP to A7 core IPC flag 2 status.  Indicates to RFDSP whether theRFTOA7 IPCFLG<2> is set.  0: The event flag is not set  1: The event flag is set |
| 1 | RFTOA7IPCFLG<1> | R | 0 | RFDSP to A7 core IPC flag 1 status.  Indicates to RFDSP whether theRFTOA7 IPCFLG<1> is set.  0: The event flag is not set  1: The event flag is set |
| 0 | RFTOA7IPCFLG<0> | R | 0 | RFDSP to A7 core IPC flag 0 status.  Indicates to RFDSP whether theRFTOA7 IPCFLG<0> is set.  0: The event flag is not set  1: The event flag is set |

### A7TORFIPCACK<15:0>

A7 core to RFDSP core IPC event acknowledge register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | A7TORFIPCACK<15> | W | 0 | A7 to RFDSP IPC event 15 acknowledge.  Writing 1 to this bit clears the A7TORFIPCFLG<15> and A7TORFIPCSTS<15> which are set by A7.  Writing 0 to this bit has no effect |
| 14 | A7TORFIPCACK<14> | W | 0 | A7 to RFDSP IPC event 14 acknowledge.  Writing 1 to this bit clears the A7TORFIPCFLG<14> and A7TORFIPCSTS<14> which are set by A7.  Writing 0 to this bit has no effect |
| 13 | A7TORFIPCACK<13> | W | 0 | A7 to RFDSP IPC event 13 acknowledge.  Writing 1 to this bit clears the A7TORFIPCFLG<13> and A7TORFIPCSTS<13> which are set by A7.  Writing 0 to this bit has no effect |
| 12 | A7TORFIPCACK<12> | W | 0 | A7 to RFDSP IPC event 12 acknowledge.  Writing 1 to this bit clears the A7TORFIPCFLG<12> and A7TORFIPCSTS<12> which are set by A7.  Writing 0 to this bit has no effect |
| 11 | A7TORFIPCACK<11> | W | 0 | A7 to RFDSP IPC event 11 acknowledge.  Writing 1 to this bit clears the A7TORFIPCFLG<11> and A7TORFIPCSTS<11> which are set by A7.  Writing 0 to this bit has no effect |
| 10 | A7TORFIPCACK<10> | W | 0 | A7 to RFDSP IPC event 10 acknowledge.  Writing 1 to this bit clears the A7TORFIPCFLG<10> and A7TORFIPCSTS<10> which are set by A7.  Writing 0 to this bit has no effect |
| 9 | A7TORFIPCACK<9 | W | 0 | A7 to RFDSP IPC event 9 acknowledge.  Writing 1 to this bit clears the A7TORFIPCFLG<9> and A7TORFIPCSTS<9> which are set by A7.  Writing 0 to this bit has no effect |
| 8 | A7TORFIPCACK<8> | W | 0 | A7 to RFDSP IPC event 8 acknowledge.  Writing 1 to this bit clears the A7TORFIPCFLG<8> and A7TORFIPCSTS<8> which are set by A7.  Writing 0 to this bit has no effect |
| 7 | A7TORFIPCACK<7> | W | 0 | A7 to RFDSP IPC event 7 acknowledge.  Writing 1 to this bit clears the A7TORFIPCFLG<7> and A7TORFIPCSTS<7> which are set by A7.  Writing 0 to this bit has no effect |
| 6 | A7TORFIPCACK<6> | W | 0 | A7 to RFDSP IPC event 6 acknowledge.  Writing 1 to this bit clears the A7TORFIPCFLG<6> and A7TORFIPCSTS<6> which are set by A7.  Writing 0 to this bit has no effect |
| 5 | A7TORFIPCACK<5> | W | 0 | A7 to RFDSP IPC event 5 acknowledge.  Writing 1 to this bit clears the A7TORFIPCFLG<5> and A7TORFIPCSTS<5> which are set by A7.  Writing 0 to this bit has no effect |
| 4 | A7TORFIPCACK<4> | W | 0 | A7 to RFDSP IPC event 4 acknowledge.  Writing 1 to this bit clears the A7TORFIPCFLG<4> and A7TORFIPCSTS<4> which are set by A7.  Writing 0 to this bit has no effect |
| 3 | A7TORFIPCACK<3> | W | 0 | A7 to RFDSP IPC event 3 acknowledge.  Writing 1 to this bit clears the A7TORFIPCFLG<3> and A7TORFIPCSTS<3> which are set by A7.  Writing 0 to this bit has no effect |
| 2 | A7TORFIPCACK<2> | W | 0 | A7 to RFDSP IPC event 2 acknowledge.  Writing 1 to this bit clears the A7TORFIPCFLG<2> and A7TORFIPCSTS<2> which are set by A7.  Writing 0 to this bit has no effect |
| 1 | A7TORFIPCACK<1> | W | 0 | A7 to RFDSP IPC event 1 acknowledge.  Writing 1 to this bit clears the A7TORFIPCFLG<1> and A7TORFIPCSTS<1> which are set by A7.  Writing 0 to this bit has no effect |
| 0 | A7TORFIPCACK<0> | W | 0 | A7 to RFDSP IPC event 0 acknowledge.  Writing 1 to this bit clears the A7TORFIPCFLG<0> and A7TORFIPCSTS<0> which are set by A7.  Writing 0 to this bit has no effect |

### A7TORFIPCSTS<15:0>

A7 core to RFDSP core IPC event status register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | A7TORFIPCSTS<15> | R | 0 | A7 to RFDSP core IPC event 15 status.  Indicates to RFDSP whether the A7TORFIPC event 15 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 14 | A7TORFIPCSTS<14> | R | 0 | A7 to RFDSP core IPC event 14 status.  Indicates to RFDSP whether the A7TORFIPC event 14 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 13 | A7TORFIPCSTS<13> | R | 0 | A7 to RFDSP core IPC event 13 status.  Indicates to RFDSP whether the A7TORFIPC event 13 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 12 | A7TORFIPCSTS<12> | R | 0 | A7 to RFDSP core IPC event 12 status.  Indicates to RFDSP whether the A7TORFIPC event 12 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 11 | A7TORFIPCSTS<11> | R | 0 | A7 to RFDSP core IPC event 11 status.  Indicates to RFDSP whether the A7TORFIPC event 11 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 10 | A7TORFIPCSTS<10> | R | 0 | A7 to RFDSP core IPC event 10 status.  Indicates to RFDSP whether the A7TORFIPC event 10 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 9 | A7TORFIPCSTS<9 | R | 0 | A7 to RFDSP core IPC event 9 status.  Indicates to RFDSP whether the A7TORFIPC event 9 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 8 | A7TORFIPCSTS<8> | R | 0 | A7 to RFDSP core IPC event 8 status.  Indicates to RFDSP whether the A7TORFIPC event 8 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 7 | A7TORFIPCSTS<7> | R | 0 | A7 to RFDSP core IPC event 7 status.  Indicates to RFDSP whether the A7TORFIPC event 7 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 6 | A7TORFIPCSTS<6> | R | 0 | A7 to RFDSP core IPC event 6 status.  Indicates to RFDSP whether the A7TORFIPC event 6 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 5 | A7TORFIPCSTS<5> | R | 0 | A7 to RFDSP core IPC event 5 status.  Indicates to RFDSP whether the A7TORFIPC event 5 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 4 | A7TORFIPCSTS<4> | R | 0 | A7 to RFDSP core IPC event 4 status.  Indicates to RFDSP whether the A7TORFIPC event 4 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 3 | A7TORFIPCSTS<3> | R | 0 | A7 to RFDSP core IPC event 3 status.  Indicates to RFDSP whether the A7TORFIPC event 3 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 2 | A7TORFIPCSTS<2> | R | 0 | A7 to RFDSP core IPC event 2 status.  Indicates to RFDSP whether the A7TORFIPC event 2 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 1 | A7TORFIPCSTS<1> | R | 0 | A7 to RFDSP core IPC event 1 status.  Indicates to RFDSP whether the A7TORFIPC event 1 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 0 | A7TORFIPCSTS<0> | R | 0 | A7 to RFDSP core IPC event 0 status.  Indicates to RFDSP whether the A7TORFIPC event 0 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |

Note: IPC event status 0-7 will trigger interrupt to the RFDSP core via the GIC.

### RFTOPLCIPCSET<15:0>

RFDSP core to PLCDSP core IPC set register

Address Offset

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | RFTOPLCIPCSET<15> | W | 0 | RFDSP to PLCDSP core IPC flag 15 set.  Writing 1 to this bit sets the RFTOPLCIPCFLG<15> for the RFDSP and RFTOPLCIPCSTS<15> for the PLCDSP.  Writing 0 has no effect. |
| 14 | RFTOPLCIPCSET<14> | W | 0 | RFDSP to PLCDSP core IPC flag 14 set.  Writing 1 to this bit sets the RFTOPLCIPCFLG<14> for the RFDSP and RFTOPLCIPCSTS<14> for the PLCDSP.  Writing 0 has no effect. |
| 13 | RFTOPLCIPCSET<13> | W | 0 | RFDSP to PLCDSP core IPC flag 13 set.  Writing 1 to this bit sets the RFTOPLCIPCFLG<13> for the RFDSP and RFTOPLCIPCSTS<13> for the PLCDSP.  Writing 0 has no effect. |
| 12 | RFTOPLCIPCSET<12> | W | 0 | RFDSP to PLCDSP core IPC flag 12 set.  Writing 1 to this bit sets the RFTOPLCIPCFLG<12> for the RFDSP and RFTOPLCIPCSTS<12> for the PLCDSP.  Writing 0 has no effect. |
| 11 | RFTOPLCIPCSET<11> | W | 0 | RFDSP to PLCDSP core IPC flag 11 set.  Writing 1 to this bit sets the RFTOPLCIPCFLG<11> for the RFDSP and RFTOPLCIPCSTS<11> for the PLCDSP.  Writing 0 has no effect. |
| 10 | RFTOPLCIPCSET<10> | W | 0 | RFDSP to PLCDSP core IPC flag 10 set.  Writing 1 to this bit sets the RFTOPLCIPCFLG<10> for the RFDSP and RFTOPLCIPCSTS<10> for the PLCDSP.  Writing 0 has no effect. |
| 9 | RFTOPLCIPCSET<9 | W | 0 | RFDSP to PLCDSP core IPC flag 9 set.  Writing 1 to this bit sets the RFTOPLCIPCFLG<9> for the RFDSP and RFTOPLCIPCSTS<9> for the PLCDSP.  Writing 0 has no effect. |
| 8 | RFTOPLCIPCSET<8> | W | 0 | RFDSP to PLCDSP core IPC flag 8 set.  Writing 1 to this bit sets the RFTOPLCIPCFLG<8> for the RFDSP and RFTOPLCIPCSTS<8> for the PLCDSP.  Writing 0 has no effect. |
| 7 | RFTOPLCIPCSET<7> | W | 0 | RFDSP to PLCDSP core IPC flag 7 set.  Writing 1 to this bit sets the RFTOPLCIPCFLG<7> for the RFDSP and RFTOPLCIPCSTS<7> for the PLCDSP.  Writing 0 has no effect. |
| 6 | RFTOPLCIPCSET<6> | W | 0 | RFDSP to PLCDSP core IPC flag 6 set.  Writing 1 to this bit sets the RFTOPLCIPCFLG<6> for the RFDSP and RFTOPLCIPCSTS<6> for the PLCDSP.  Writing 0 has no effect. |
| 5 | RFTOPLCIPCSET<5> | W | 0 | RFDSP to PLCDSP core IPC flag 5 set.  Writing 1 to this bit sets the RFTOPLCIPCFLG<5> for the RFDSP and RFTOPLCIPCSTS<5> for the PLCDSP.  Writing 0 has no effect. |
| 4 | RFTOPLCIPCSET<4> | W | 0 | RFDSP to PLCDSP core IPC flag 4 set.  Writing 1 to this bit sets the RFTOPLCIPCFLG<4> for the RFDSP and RFTOPLCIPCSTS<4> for the PLCDSP.  Writing 0 has no effect. |
| 3 | RFTOPLCIPCSET<3> | W | 0 | RFDSP to PLCDSP core IPC flag 3 set.  Writing 1 to this bit sets the RFTOPLCIPCFLG<3> for the RFDSP and RFTOPLCIPCSTS<3> for the PLCDSP.  Writing 0 has no effect. |
| 2 | RFTOPLCIPCSET<2> | W | 0 | RFDSP to PLCDSP core IPC flag 2 set.  Writing 1 to this bit sets the RFTOPLCIPCFLG<2> for the RFDSP and RFTOPLCIPCSTS<2> for the PLCDSP.  Writing 0 has no effect. |
| 1 | RFTOPLCIPCSET<1> | W | 0 | RFDSP to PLCDSP core IPC flag 1 set.  Writing 1 to this bit sets the RFTOPLCIPCFLG<1> for the RFDSP and RFTOPLCIPCSTS<1> for the PLCDSP.  Writing 0 has no effect. |
| 0 | RFTOPLCIPCSET<0> | W | 0 | RFDSP to PLCDSP core IPC flag 0 set.  Writing 1 to this bit sets the RFTOPLCIPCFLG<0> for the RFDSP and RFTOPLCIPCSTS<0> for the PLCDSP.  Writing 0 has no effect. |

### RFTOPLCIPCCLR<15:0>

RFDSP core to PLCDSP core IPC clear register

Address Offset

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | RFTOPLCIPCCLR<15> | W | 0 | RFDSP to PLCDSP core IPC flag 15 clear.  Writing 1 to this bit clears the RFTOPLCIPCFLG<15> for the RFDSP and RFTOPLCIPCSTS<15> for the PLCDSP.  Writing 0 has no effect. |
| 14 | RFTOPLCIPCCLR<14> | W | 0 | RFDSP to PLCDSP core IPC flag 14 clear.  Writing 1 to this bit clears the RFTOPLCIPCFLG<14> for the RFDSP and RFTOPLCIPCSTS<14> for the PLCDSP.  Writing 0 has no effect. |
| 13 | RFTOPLCIPCCLR<13> | W | 0 | RFDSP to PLCDSP core IPC flag 13 clear.  Writing 1 to this bit clears the RFTOPLCIPCFLG<13> for the RFDSP and RFTOPLCIPCSTS<13> for the PLCDSP.  Writing 0 has no effect. |
| 12 | RFTOPLCIPCCLR<12> | W | 0 | RFDSP to PLCDSP core IPC flag 12 clear.  Writing 1 to this bit clears the RFTOPLCIPCFLG<12> for the RFDSP and RFTOPLCIPCSTS<12> for the PLCDSP.  Writing 0 has no effect. |
| 11 | RFTOPLCIPCCLR<11> | W | 0 | RFDSP to PLCDSP core IPC flag 11 clear.  Writing 1 to this bit clears the RFTOPLCIPCFLG<11> for the RFDSP and RFTOPLCIPCSTS<11> for the PLCDSP.  Writing 0 has no effect. |
| 10 | RFTOPLCIPCCLR<10> | W | 0 | RFDSP to PLCDSP core IPC flag 10 clear.  Writing 1 to this bit clears the RFTOPLCIPCFLG<10> for the RFDSP and RFTOPLCIPCSTS<10> for the PLCDSP.  Writing 0 has no effect. |
| 9 | RFTOPLCIPCCLR<9 | W | 0 | RFDSP to PLCDSP core IPC flag 9 clear.  Writing 1 to this bit clears the RFTOPLCIPCFLG<9> for the RFDSP and RFTOPLCIPCSTS<9> for the PLCDSP.  Writing 0 has no effect. |
| 8 | RFTOPLCIPCCLR<8> | W | 0 | RFDSP to PLCDSP core IPC flag 8 clear.  Writing 1 to this bit clears the RFTOPLCIPCFLG<8> for the RFDSP and RFTOPLCIPCSTS<8> for the PLCDSP.  Writing 0 has no effect. |
| 7 | RFTOPLCIPCCLR<7> | W | 0 | RFDSP to PLCDSP core IPC flag 7 clear.  Writing 1 to this bit clears the RFTOPLCIPCFLG<7> for the RFDSP and RFTOPLCIPCSTS<7> for the PLCDSP.  Writing 0 has no effect. |
| 6 | RFTOPLCIPCCLR<6> | W | 0 | RFDSP to PLCDSP core IPC flag 6 clear.  Writing 1 to this bit clears the RFTOPLCIPCFLG<6> for the RFDSP and RFTOPLCIPCSTS<6> for the PLCDSP.  Writing 0 has no effect. |
| 5 | RFTOPLCIPCCLR<5> | W | 0 | RFDSP to PLCDSP core IPC flag 5 clear.  Writing 1 to this bit clears the RFTOPLCIPCFLG<5> for the RFDSP and RFTOPLCIPCSTS<5> for the PLCDSP.  Writing 0 has no effect. |
| 4 | RFTOPLCIPCCLR<4> | W | 0 | RFDSP to PLCDSP core IPC flag 4 clear.  Writing 1 to this bit clears the RFTOPLCIPCFLG<4> for the RFDSP and RFTOPLCIPCSTS<4> for the PLCDSP.  Writing 0 has no effect. |
| 3 | RFTOPLCIPCCLR<3> | W | 0 | RFDSP to PLCDSP core IPC flag 3 clear.  Writing 1 to this bit clears the RFTOPLCIPCFLG<3> for the RFDSP and RFTOPLCIPCSTS<3> for the PLCDSP.  Writing 0 has no effect. |
| 2 | RFTOPLCIPCCLR<2> | W | 0 | RFDSP to PLCDSP core IPC flag 2 clear.  Writing 1 to this bit clears the RFTOPLCIPCFLG<2> for the RFDSP and RFTOPLCIPCSTS<2> for the PLCDSP.  Writing 0 has no effect. |
| 1 | RFTOPLCIPCCLR<1> | W | 0 | RFDSP to PLCDSP core IPC flag 1 clear.  Writing 1 to this bit clears the RFTOPLCIPCFLG<1> for the RFDSP and RFTOPLCIPCSTS<1> for the PLCDSP.  Writing 0 has no effect. |
| 0 | RFTOPLCIPCCLR<0> | W | 0 | RFDSP to PLCDSP core IPC flag 0 clear.  Writing 1 to this bit clears the RFTOPLCIPCFLG<0> for the RFDSP and RFTOPLCIPCSTS<0> for the PLCDSP.  Writing 0 has no effect. |

Notes: Normally, PLCDSP will clear (acknowledge) the RFtoPLC IPC event flags. This mechanism may be useful if PLC DSP is non-responsive.

### RFTOPLCIPCFLG<15:0>

RFDSP core to PLCDSP core IPC flags register

Address Offset

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | RFTOPLCIPCFLG<15> | R | 0 | RFDSP to PLCDSP core IPC flag 15 status.  Indicates to RFDSP whether the RFTOPLCIPCFLG<15> is set.  0: The event flag is not set  1: The event flag is set |
| 14 | RFTOPLCIPCFLG<14> | R | 0 | RFDSP to PLCDSP core IPC flag 14 status.  Indicates to RFDSP whether the RFTOPLCIPCFLG<14> is set.  0: The event flag is not set  1: The event flag is set |
| 13 | RFTOPLCIPCFLG<13> | R | 0 | RFDSP to PLCDSP core IPC flag 13 status.  Indicates to RFDSP whether the RFTOPLCIPCFLG<13> is set.  0: The event flag is not set  1: The event flag is set |
| 12 | RFTOPLCIPCFLG<12> | R | 0 | RFDSP to PLCDSP core IPC flag 12 status.  Indicates to RFDSP whether the RFTOPLCIPCFLG<12> is set.  0: The event flag is not set  1: The event flag is set |
| 11 | RFTOPLCIPCFLG<11> | R | 0 | RFDSP to PLCDSP core IPC flag 11 status.  Indicates to RFDSP whether the RFTOPLCIPCFLG<11> is set.  0: The event flag is not set  1: The event flag is set |
| 10 | RFTOPLCIPCFLG<10> | R | 0 | RFDSP to PLCDSP core IPC flag 10 status.  Indicates to RFDSP whether the RFTOPLCIPCFLG<10> is set.  0: The event flag is not set  1: The event flag is set |
| 9 | RFTOPLCIPCFLG<9 | R | 0 | RFDSP to PLCDSP core IPC flag 9 status.  Indicates to RFDSP whether the RFTOPLCIPCFLG<9> is set.  0: The event flag is not set  1: The event flag is set |
| 8 | RFTOPLCIPCFLG<8> | R | 0 | RFDSP to PLCDSP core IPC flag 8 status.  Indicates to RFDSP whether the RFTOPLCIPCFLG<8> is set.  0: The event flag is not set  1: The event flag is set |
| 7 | RFTOPLCIPCFLG<7> | R | 0 | RFDSP to PLCDSP core IPC flag 7 status.  Indicates to RFDSP whether the RFTOPLCIPCFLG<7> is set.  0: The event flag is not set  1: The event flag is set |
| 6 | RFTOPLCIPCFLG<6> | R | 0 | RFDSP to PLCDSP core IPC flag 6 status.  Indicates to RFDSP whether the RFTOPLCIPCFLG<6> is set.  0: The event flag is not set  1: The event flag is set |
| 5 | RFTOPLCIPCFLG<5> | R | 0 | RFDSP to PLCDSP core IPC flag 5 status.  Indicates to RFDSP whether the RFTOPLCIPCFLG<5> is set.  0: The event flag is not set  1: The event flag is set |
| 4 | RFTOPLCIPCFLG<4> | R | 0 | RFDSP to PLCDSP core IPC flag 4 status.  Indicates to RFDSP whether the RFTOPLCIPCFLG<4> is set.  0: The event flag is not set  1: The event flag is set |
| 3 | RFTOPLCIPCFLG<3> | R | 0 | RFDSP to PLCDSP core IPC flag 3 status.  Indicates to RFDSP whether the RFTOPLCIPCFLG<3> is set.  0: The event flag is not set  1: The event flag is set |
| 2 | RFTOPLCIPCFLG<2> | R | 0 | RFDSP to PLCDSP core IPC flag 2 status.  Indicates to RFDSP whether the RFTOPLCIPCFLG<2> is set.  0: The event flag is not set  1: The event flag is set |
| 1 | RFTOPLCIPCFLG<1> | R | 0 | RFDSP to PLCDSP core IPC flag 1 status.  Indicates to RFDSP whether the RFTOPLCIPCFLG<1> is set.  0: The event flag is not set  1: The event flag is set |
| 0 | RFTOPLCIPCFLG<0> | R | 0 | RFDSP to PLCDSP core IPC flag 0 status.  Indicates to RFDSP whether the RFTOPLCIPCFLG<0> is set.  0: The event flag is not set  1: The event flag is set |

### PLCTORFIPCACK<15:0>

PLCDSP core to RFDSP core IPC event acknowledge register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | PLCTORFIPCACK<15> | W | 0 | PLCDSP to RFDSP IPC event 15 acknowledge.  Writing 1 to this bit clears the PLCTORFIPCFLG<15> and PLCTORFIPCSTS<15> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 14 | PLCTORFIPCACK<14> | W | 0 | PLCDSP to RFDSP IPC event 14 acknowledge.  Writing 1 to this bit clears the PLCTORFIPCFLG<14> and PLCTORFIPCSTS<14> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 13 | PLCTORFIPCACK<13> | W | 0 | PLCDSP to RFDSP IPC event 13 acknowledge.  Writing 1 to this bit clears the PLCTORFIPCFLG<13> and PLCTORFIPCSTS<13> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 12 | PLCTORFIPCACK<12> | W | 0 | PLCDSP to RFDSP IPC event 12 acknowledge.  Writing 1 to this bit clears the PLCTORFIPCFLG<12> and PLCTORFIPCSTS<12> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 11 | PLCTORFIPCACK<11> | W | 0 | PLCDSP to RFDSP IPC event 11 acknowledge.  Writing 1 to this bit clears the PLCTORFIPCFLG<11> and PLCTORFIPCSTS<11> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 10 | PLCTORFIPCACK<10> | W | 0 | PLCDSP to RFDSP IPC event 10 acknowledge.  Writing 1 to this bit clears the PLCTORFIPCFLG<10> and PLCTORFIPCSTS<10> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 9 | PLCTORFIPCACK<9 | W | 0 | PLCDSP to RFDSP IPC event 9 acknowledge.  Writing 1 to this bit clears the PLCTORFIPCFLG<9> and PLCTORFIPCSTS<9> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 8 | PLCTORFIPCACK<8> | W | 0 | PLCDSP to RFDSP IPC event 8 acknowledge.  Writing 1 to this bit clears the PLCTORFIPCFLG<8> and PLCTORFIPCSTS<8> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 7 | PLCTORFIPCACK<7> | W | 0 | PLCDSP to RFDSP IPC event 7 acknowledge.  Writing 1 to this bit clears the PLCTORFIPCFLG<7> and PLCTORFIPCSTS<7> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 6 | PLCTORFIPCACK<6> | W | 0 | PLCDSP to RFDSP IPC event 6 acknowledge.  Writing 1 to this bit clears the PLCTORFIPCFLG<6> and PLCTORFIPCSTS<6> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 5 | PLCTORFIPCACK<5> | W | 0 | PLCDSP to RFDSP IPC event 5 acknowledge.  Writing 1 to this bit clears the PLCTORFIPCFLG<5> and PLCTORFIPCSTS<5> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 4 | PLCTORFIPCACK<4> | W | 0 | PLCDSP to RFDSP IPC event 4 acknowledge.  Writing 1 to this bit clears the PLCTORFIPCFLG<4> and PLCTORFIPCSTS<4> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 3 | PLCTORFIPCACK<3> | W | 0 | PLCDSP to RFDSP IPC event 3 acknowledge.  Writing 1 to this bit clears the PLCTORFIPCFLG<3> and PLCTORFIPCSTS<3> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 2 | PLCTORFIPCACK<2> | W | 0 | PLCDSP to RFDSP IPC event 2 acknowledge.  Writing 1 to this bit clears the PLCTORFIPCFLG<2> and PLCTORFIPCSTS<2> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 1 | PLCTORFIPCACK<1> | W | 0 | PLCDSP to RFDSP IPC event 1 acknowledge.  Writing 1 to this bit clears the PLCTORFIPCFLG<1> and PLCTORFIPCSTS<1> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 0 | PLCTORFIPCACK<0> | W | 0 | PLCDSP to RFDSP IPC event 0 acknowledge.  Writing 1 to this bit clears the PLCTORFIPCFLG<0> and PLCTORFIPCSTS<0> which are set by PLCDSP.  Writing 0 to this bit has no effect |

### PLCTORFIPCSTS<15:0>

PLCDSP core to RFDSP core IPC event status register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | PLCTORFIPCSTS<15> | R | 0 | PLCDSP to RFDSP core IPC event 15 status.  Indicates to RFDSP whether the PLCTORFIPC event 15 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 14 | PLCTORFIPCSTS<14> | R | 0 | PLCDSP to RFDSP core IPC event 14 status.  Indicates to RFDSP whether the PLCTORFIPC event 14 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 13 | PLCTORFIPCSTS<13> | R | 0 | PLCDSP to RFDSP core IPC event 13 status.  Indicates to RFDSP whether the PLCTORFIPC event 13 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 12 | PLCTORFIPCSTS<12> | R | 0 | PLCDSP to RFDSP core IPC event 12 status.  Indicates to RFDSP whether the PLCTORFIPC event 12 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 11 | PLCTORFIPCSTS<11> | R | 0 | PLCDSP to RFDSP core IPC event 11 status.  Indicates to RFDSP whether the PLCTORFIPC event 11 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 10 | PLCTORFIPCSTS<10> | R | 0 | PLCDSP to RFDSP core IPC event 10 status.  Indicates to RFDSP whether the PLCTORFIPC event 10 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 9 | PLCTORFIPCSTS<9 | R | 0 | PLCDSP to RFDSP core IPC event 9 status.  Indicates to RFDSP whether the PLCTORFIPC event 9 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 8 | PLCTORFIPCSTS<8> | R | 0 | PLCDSP to RFDSP core IPC event 8 status.  Indicates to RFDSP whether the PLCTORFIPC event 8 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 7 | PLCTORFIPCSTS<7> | R | 0 | PLCDSP to RFDSP core IPC event 7 status.  Indicates to RFDSP whether the PLCTORFIPC event 7 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 6 | PLCTORFIPCSTS<6> | R | 0 | PLCDSP to RFDSP core IPC event 6 status.  Indicates to RFDSP whether the PLCTORFIPC event 6 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 5 | PLCTORFIPCSTS<5> | R | 0 | PLCDSP to RFDSP core IPC event 5 status.  Indicates to RFDSP whether the PLCTORFIPC event 5 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 4 | PLCTORFIPCSTS<4> | R | 0 | PLCDSP to RFDSP core IPC event 4 status.  Indicates to RFDSP whether the PLCTORFIPC event 4 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 3 | PLCTORFIPCSTS<3> | R | 0 | PLCDSP to RFDSP core IPC event 3 status.  Indicates to RFDSP whether the PLCTORFIPC event 3 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 2 | PLCTORFIPCSTS<2> | R | 0 | PLCDSP to RFDSP core IPC event 2 status.  Indicates to RFDSP whether the PLCTORFIPC event 2 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 1 | PLCTORFIPCSTS<1> | R | 0 | PLCDSP to RFDSP core IPC event 1 status.  Indicates to RFDSP whether the PLCTORFIPC event 1 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 0 | PLCTORFIPCSTS<0> | R | 0 | PLCDSP to RFDSP core IPC event 0 status.  Indicates to RFDSP whether the PLCTORFIPC event 0 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |

Note: IPC event status 0-7 will trigger interrupt to the RFDSP core via the GIC.

### A7TORFIPCTEST<31:0>

A7 To RF Interrupt test register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:8 | reserved |  |  | Reserved |
| 7:0 | A7TORFIPCTEST | R/W | 0 | To force IPC\_A7TORF\_INT to be triggered, it is for debugging purpose only.  When write 1 to any bit of A7TORFIPCTEST, corresponding bit on IPC\_A7TORF\_INT[7:0] is asserted  When write 0, A7TORFIPCTEST has no effect on IPC\_A7TORF\_INT[7:0] |

### PLCTORFIPCTEST<31:0>

PLC To RF Interrupt test register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:8 | reserved |  |  | Reserved |
| 7:0 | PLCTORFIPCTEST | R/W | 0 | To force IPC\_PLCTORF\_INT to be triggered, it is for debugging purpose only.  When write 1 to any bit of PLCTORFIPCTEST, corresponding bit on IPC\_PLCTORF\_INT[7:0] is asserted  When write 0, PLCTORFIPCTEST has no effect on IPC\_PLCTORF\_INT[7:0] |

### PLCTORFACK\_INT\_CLR<31:0>

PLC to RF ACK interrupt clear register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:1 | reserved |  |  | Reserved |
| 0 | PLCTORFACK\_INT\_CLR | W | 0 | To clear PLC to RF ACK interrupt flag  When write 1, PLCTORF\_ACK\_INT is cleared |

### A7TORFACK\_INT\_CLR<31:0>

A7 to RF ACK interrupt clear register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:1 | reserved |  |  | Reserved |
| 0 | A7TORFACK\_INT\_CLR | W | 0 | To clear A7 to RF ACK interrupt flag  When write 1, A7TORF\_ACK\_INT is cleared |

### RFSRP00REQ<31:0>

Shared RAM page0 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 0 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP01REQ<31:0>

Shared RAM page1 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 1 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP02REQ<31:0>

Shared RAM page2 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 2 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP03REQ<31:0>

Shared RAM page3 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 3 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP04REQ<31:0>

Shared RAM page4 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page4 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP05REQ<31:0>

Shared RAM page5 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 5 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP06REQ<31:0>

Shared RAM page6 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 6 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP07REQ<31:0>

Shared RAM page7 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page7 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP08REQ<31:0>

Shared RAM page8 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 8 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP09REQ<31:0>

Shared RAM page9 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 9 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP10REQ<31:0>

Shared RAM page10 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page1 0 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP11REQ<31:0>

Shared RAM page11 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 11 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP12REQ<31:0>

Shared RAM page12 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 12 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP13REQ<31:0>

Shared RAM page13 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 13 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP14REQ<31:0>

Shared RAM page14 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 14 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP15REQ<31:0>

Shared RAM page15 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page15 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP16REQ<31:0>

Shared RAM page16 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 16 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP17REQ<31:0>

Shared RAM page17 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page17 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP18REQ<31:0>

Shared RAM page18 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 18 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP19REQ<31:0>

Shared RAM page19 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 19 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP20REQ<31:0>

Shared RAM page20 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 20 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP21REQ<31:0>

Shared RAM page21 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 21 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP22REQ<31:0>

Shared RAM page22 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 22 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP23REQ<31:0>

Shared RAM page23 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 23 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP24REQ<31:0>

Shared RAM page24 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 24 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP25REQ<31:0>

Shared RAM page25 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 25 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP26REQ<31:0>

Shared RAM page26 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 26 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP27REQ<31:0>

Shared RAM page27 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 27 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP28REQ<31:0>

Shared RAM page28 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 28 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP29REQ<31:0>

Shared RAM page29 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 29 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP30REQ<31:0>

Shared RAM page30 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 30 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### RFSRP31REQ<31:0>

Shared RAM page31 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x3589BCD will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 31 write access request semaphore from RFDSP:  Write a value “10” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLC DSP core IPC registers

### A7TOPLCIPCCOMM<31:0>

A7 core to PLCDSP core IPC command register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | COMMAND | R | 0 | This is a general purpose register used to send software-defined commands from A7 to PLCDSP. |

### A7TOPLCIPCADDR<31:0>

A7 core to PLCDSP core IPC address register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | ADDRESS | R | 0 | This is a general purpose register used to send software-defined address from A7 to PLCDSP. |

### A7TOPLCIPCDATA0<31:0>

A7 core to PLCDSP core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA0 | R | 0 | This is a general purpose register used to send software-defined data from A7 to PLCDSP. |

### A7TOPLCIPCDATA1<31:0>

A7 core to PLCDSP core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA1 | R- | 0 | This is a general purpose register used to send software-defined data from A7 to PLCDSP. |

### RFTOPLCIPCCOMM<31:0>

RFDSP core to PLCDSP core IPC command register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | COMMAND | R | 0 | This is a general purpose register used to send software-defined commands from RFDSP to PLCDSP. |

### RFTOPLCIPCADDR<31:0>

RFDSP core to PLCDSP core IPC address register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | ADDRESS | R | 0 | This is a general purpose register used to send software-defined address from RFDSP to PLCDSP. |

### RFTOPLCIPCDATA0<31:0>

RFDSP core to PLCDSP core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA0 | R | 0 | This is a general purpose register used to send software-defined data from RFDSP to PLCDSP. |

### RFTOPLCIPCDATA1<31:0>

RFDSP core to PLCDSP core IPC response register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA1 | R | 0 | This is a general purpose register used to send software-defined data from RFDSP to PLCDSP. |

### PLCTOA7IPCCOMM<31:0>

PLCDSP core to A7 core IPC command register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | COMMAND | R/W | 0 | This is a general purpose register used to send software-defined commands from PLCDSP to A7. |

### PLCTOA7IPCADDR<31:0>

PLCDSP core to A7 core IPC address register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | ADDRESS | R/W | 0 | This is a general purpose register used to send software-defined address from PLCDSP to A7. |

### PLCTOA7IPCDATA0<31:0>

PLCDSP core to A7 core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA0 | R/W | 0 | This is a general purpose register used to send software-defined data from PLCDSP to A7. |

### PLCTOA7IPCDATA1<31:0>

PLCDSP core to A7 core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA1 | R/W | 0 | This is a general purpose register used to to send software-defined data from PLCDSP to A7. |

### PLCTORFIPCCOMM<31:0>

PLCDSP core to RFDSP core IPC command register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | COMMAND | R/W | 0 | This is a general purpose register used to send software-defined commands from PLCDSP to RFDSP. |

### PLCTORFIPCADDR<31:0>

PLCDSP core to RFDSP core IPC address register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | ADDRESS | R/W | 0 | This is a general purpose register used to send software-defined address from PLCDSP to RFDSP. |

### PLCTORFIPCDATA0<31:0>

PLCDSP core to RFDSP core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA0 | R/W | 0 | This is a general purpose register used to send software-defined data from PLCDSP to RFDSP. |

### PLCTORFIPCDATA1<31:0>

PLCDSP core to RFDSP core IPC data register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | WDATA1 | R/W | 0 | This is a general purpose register used to send software-defined data from PLCDSP to RFDSP. |

### IPCTMRSCALER <31:0>

Free running 64bit timestamp counter prescaler register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15:0 | PRESCALER | R | 0 | The prescaler value used to derive the free running timer’s clock: Ftimer=Fcpu/(prescaler+1).  Prescale counter is reset whenever this setting or IPCTMRCNT is changed  It can be only configured by RF Core |

### IPCCOUNTERL <31:0>

Free running 64bit timestamp counter low register.

To ensure the integrity of read data from AHB bus, a snapshot for the high 32-bits counter is taken when a read is performed on the IPCCOUNTERL register. When the PLC DSP core reads the IPCOUNTERH, the snapshot is fed back to the user instead of the current value in the IPCOUNTERH register. Therefore, the user application software must always read IPCCOUNTERL first and then read IPCCOUNTERH.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | IPCCOUNTERL | R | 0 | This is the lower 32-bits of free running 64 bit timestamp counter clocked by the divided clock. |

### IPCCOUNTERH <31:0>

Free running 64bit timestamp counter high register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | IPCCOUNTERH | R | 0 | This is the upper 32-bits of free running 64 bit timestamp counter clocked by the divided clock. |

### IPCTMRCONT <31:0>

Free running 64bit control register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:1 | Reserved |  |  |  |
| 0 | TMRCOUNTUP | R | 1 | 0x1: Timer as upward counter  0x0: Timer as downward counter  It can be only configured by RF Core  Timer count value is reset to 0x0 (count up) or 0xffffffff\_ffffffff (count down) whenever TMRCOUNTUP setting is changed |

### SRMSEL0<31:0>

Shared RAM pages’ ownership (master selection) status register0

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:30 | SRP15OWN | R | 0 | Shared RAM page15 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 29:28 | SRP14OWN | R | 0 | Shared RAM page 14 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 27:26 | SRP13OWN | R | 0 | Shared RAM page 13 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 25:24 | SRP12OWN | R | 0 | Shared RAM page 12 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 23:22 | SRP110OWN | R | 0 | Shared RAM page 11 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 21:20 | SRP10OWN | R | 0 | Shared RAM page 10 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 19:18 | SRP09OWN | R | 0 | Shared RAM page 9 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 17:16 | SRP08OWN | R | 0 | Shared RAM page 8 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 15:14 | SRP07OWN | R | 0 | Shared RAM page 7 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 13:12 | SRP06OWN | R | 0 | Shared RAM page 6 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 11:10 | SRP05OWN | R | 0 | Shared RAM page 5 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 9:8 | SRP04OWN | R | 0 | Shared RAM page 4 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 7:6 | SRP03OWN | R | 0 | Shared RAM page 3 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 5:4 | SRP02OWN | R | 0 | Shared RAM page 2 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 3:2 | SRP01OWN | R | 0 | Shared RAM page 1 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 1:0 | SRP00OWN | R | 0 | Shared RAM page 0 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |

### SRMSEL1<31:0>

Shared RAM pages’ ownership (master selection) status register1

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:30 | SRP31OWN | R | 0 | Shared RAM page 31 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 29:28 | SRP30OWN | R | 0 | Shared RAM page 30 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 27:26 | SRP29OWN | R | 0 | Shared RAM page 29 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 25:24 | SRP28OWN | R | 0 | Shared RAM page 28 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 23:22 | SRP270OWN | R | 0 | Shared RAM page 27 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 21:20 | SRP26OWN | R | 0 | Shared RAM page 26 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 19:18 | SRP25OWN | R | 0 | Shared RAM page 25 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 17:16 | SRP24OWN | R | 0 | Shared RAM page 24 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 15:14 | SRP23OWN | R | 0 | Shared RAM page 23 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 13:12 | SRP22OWN | R | 0 | Shared RAM page 22 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 11:10 | SRP21OWN | R | 0 | Shared RAM page 21 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 9:8 | SRP20OWN | R | 0 | Shared RAM page 20 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 7:6 | SRP19OWN | R | 0 | Shared RAM page 19 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 5:4 | SRP18OWN | R | 0 | Shared RAM page 18 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 3:2 | SRP17OWN | R | 0 | Shared RAM page 17 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |
| 1:0 | SRP16OWN | R | 0 | Shared RAM page 16 ownership status:  00: no owner; 01: owned by A7;  10: owned by RFDSP; 11: owned by PLCDSP. |

### PLCTOA7IPCSET<15:0>

PLCDSP core to A7 core IPC set register

Address Offset

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | PLCTOA7IPCSET<15> | W | 0 | PLCDSP to A7 core IPC flag 15 set.  Writing 1 to this bit sets the PLCTOA7IPCFLG<15> for the PLCDSP and PLCTOA7IPCSTS<15> for the A7.  Writing 0 has no effect. |
| 14 | PLCTOA7IPCSET<14> | W | 0 | PLCDSP to A7 core IPC flag 14 set.  Writing 1 to this bit sets the PLCTOA7IPCFLG<14> for the PLCDSP and PLCTOA7IPCSTS<14> for the A7.  Writing 0 has no effect. |
| 13 | PLCTOA7IPCSET<13> | W | 0 | PLCDSP to A7 core IPC flag 13 set.  Writing 1 to this bit sets the PLCTOA7IPCFLG<13> for the PLCDSP and PLCTOA7IPCSTS<13> for the A7.  Writing 0 has no effect. |
| 12 | PLCTOA7IPCSET<12> | W | 0 | PLCDSP to A7 core IPC flag 12 set.  Writing 1 to this bit sets the PLCTOA7IPCFLG<12> for the PLCDSP and PLCTOA7IPCSTS<12> for the A7.  Writing 0 has no effect. |
| 11 | PLCTOA7IPCSET<11> | W | 0 | PLCDSP to A7 core IPC flag 11 set.  Writing 1 to this bit sets the PLCTOA7IPCFLG<11> for the PLCDSP and PLCTOA7IPCSTS<11> for the A7.  Writing 0 has no effect. |
| 10 | PLCTOA7IPCSET<10> | W | 0 | PLCDSP to A7 core IPC flag 10 set.  Writing 1 to this bit sets the PLCTOA7IPCFLG<10> for the PLCDSP and PLCTOA7IPCSTS<10> for the A7.  Writing 0 has no effect. |
| 9 | PLCTOA7IPCSET<9 | W | 0 | PLCDSP to A7 core IPC flag 9 set.  Writing 1 to this bit sets the PLCTOA7IPCFLG<9> for the PLCDSP and PLCTOA7IPCSTS<9> for the A7.  Writing 0 has no effect. |
| 8 | PLCTOA7IPCSET<8> | W | 0 | PLCDSP to A7 core IPC flag 8 set.  Writing 1 to this bit sets the PLCTOA7IPCFLG<8> for the PLCDSP and PLCTOA7IPCSTS<8> for the A7.  Writing 0 has no effect. |
| 7 | PLCTOA7IPCSET<7> | W | 0 | PLCDSP to A7 core IPC flag 7 set.  Writing 1 to this bit sets the PLCTOA7IPCFLG<7> for the PLCDSP and PLCTOA7IPCSTS<7> for the A7.  Writing 0 has no effect. |
| 6 | PLCTOA7IPCSET<6> | W | 0 | PLCDSP to A7 core IPC flag 6 set.  Writing 1 to this bit sets the PLCTOA7IPCFLG<6> for the PLCDSP and PLCTOA7IPCSTS<6> for the A7.  Writing 0 has no effect. |
| 5 | PLCTOA7IPCSET<5> | W | 0 | PLCDSP to A7 core IPC flag 5 set.  Writing 1 to this bit sets the PLCTOA7IPCFLG<5> for the PLCDSP and PLCTOA7IPCSTS<5> for the A7.  Writing 0 has no effect. |
| 4 | PLCTOA7IPCSET<4> | W | 0 | PLCDSP to A7 core IPC flag 4 set.  Writing 1 to this bit sets the PLCTOA7IPCFLG<4> for the PLCDSP and PLCTOA7IPCSTS<4> for the A7.  Writing 0 has no effect. |
| 3 | PLCTOA7IPCSET<3> | W | 0 | PLCDSP to A7 core IPC flag 3 set.  Writing 1 to this bit sets the PLCTOA7IPCFLG<3> for the PLCDSP and PLCTOA7IPCSTS<3> for the A7.  Writing 0 has no effect. |
| 2 | PLCTOA7IPCSET<2> | W | 0 | PLCDSP to A7 core IPC flag 2 set.  Writing 1 to this bit sets the PLCTOA7IPCFLG<2> for the PLCDSP and PLCTOA7IPCSTS<2> for the A7.  Writing 0 has no effect. |
| 1 | PLCTOA7IPCSET<1> | W | 0 | PLCDSP to A7 core IPC flag 1 set.  Writing 1 to this bit sets the PLCTOA7IPCFLG<1> for the PLCDSP and PLCTOA7IPCSTS<1> for the A7.  Writing 0 has no effect. |
| 0 | PLCTOA7IPCSET<0> | W | 0 | PLCDSP to A7 core IPC flag 0 set.  Writing 1 to this bit sets the PLCTOA7IPCFLG<0> for the PLCDSP and PLCTOA7IPCSTS<0> for the A7.  Writing 0 has no effect. |

### PLCTOA7IPCCLR<15:0>

PLCDSP core to A7 core IPC clear register

Address Offset

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | PLCTOA7IPCCLR<15> | W | 0 | PLCDSP to A7 core IPC flag 15 clear.  Writing 1 to this bit clears the PLCTOA7IPCFLG<15> for the PLCDSP and PLCTOA7IPCSTS<15> for the A7.  Writing 0 has no effect. |
| 14 | PLCTOA7IPCCLR<14> | W | 0 | PLCDSP to A7 core IPC flag 14 clear.  Writing 1 to this bit clears the PLCTOA7IPCFLG<14> for the PLCDSP and PLCTOA7IPCSTS<14> for the A7.  Writing 0 has no effect. |
| 13 | PLCTOA7IPCCLR<13> | W | 0 | PLCDSP to A7 core IPC flag 13 clear.  Writing 1 to this bit clears the PLCTOA7IPCFLG<13> for the PLCDSP and PLCTOA7IPCSTS<13> for the A7.  Writing 0 has no effect. |
| 12 | PLCTOA7IPCCLR<12> | W | 0 | PLCDSP to A7 core IPC flag 12 clear.  Writing 1 to this bit clears the PLCTOA7IPCFLG<12> for the PLCDSP and PLCTOA7IPCSTS<12> for the A7.  Writing 0 has no effect. |
| 11 | PLCTOA7IPCCLR<11> | W | 0 | PLCDSP to A7 core IPC flag 11 clear.  Writing 1 to this bit clears the PLCTOA7IPCFLG<11> for the PLCDSP and PLCTOA7IPCSTS<11> for the A7.  Writing 0 has no effect. |
| 10 | PLCTOA7IPCCLR<10> | W | 0 | PLCDSP to A7 core IPC flag 10 clear.  Writing 1 to this bit clears the PLCTOA7IPCFLG<10> for the PLCDSP and PLCTOA7IPCSTS<10> for the A7.  Writing 0 has no effect. |
| 9 | PLCTOA7IPCCLR<9 | W | 0 | PLCDSP to A7 core IPC flag 9 clear.  Writing 1 to this bit clears the PLCTOA7IPCFLG<9> for the PLCDSP and PLCTOA7IPCSTS<9> for the A7.  Writing 0 has no effect. |
| 8 | PLCTOA7IPCCLR<8> | W | 0 | PLCDSP to A7 core IPC flag 8 clear.  Writing 1 to this bit clears the PLCTOA7IPCFLG<8> for the PLCDSP and PLCTOA7IPCSTS<8> for the A7.  Writing 0 has no effect. |
| 7 | PLCTOA7IPCCLR<7> | W | 0 | PLCDSP to A7 core IPC flag 7 clear.  Writing 1 to this bit clears the PLCTOA7IPCFLG<7> for the PLCDSP and PLCTOA7IPCSTS<7> for the A7.  Writing 0 has no effect. |
| 6 | PLCTOA7IPCCLR<6> | W | 0 | PLCDSP to A7 core IPC flag 6 clear.  Writing 1 to this bit clears the PLCTOA7IPCFLG<6> for the PLCDSP and PLCTOA7IPCSTS<6> for the A7.  Writing 0 has no effect. |
| 5 | PLCTOA7IPCCLR<5> | W | 0 | PLCDSP to A7 core IPC flag 5 clear.  Writing 1 to this bit clears the PLCTOA7IPCFLG<5> for the PLCDSP and PLCTOA7IPCSTS<5> for the A7.  Writing 0 has no effect. |
| 4 | PLCTOA7IPCCLR<4> | W | 0 | PLCDSP to A7 core IPC flag 4 clear.  Writing 1 to this bit clears the PLCTOA7IPCFLG<4> for the PLCDSP and PLCTOA7IPCSTS<4> for the A7.  Writing 0 has no effect. |
| 3 | PLCTOA7IPCCLR<3> | W | 0 | PLCDSP to A7 core IPC flag 3 clear.  Writing 1 to this bit clears the PLCTOA7IPCFLG<3> for the PLCDSP and PLCTOA7IPCSTS<3> for the A7.  Writing 0 has no effect. |
| 2 | PLCTOA7IPCCLR<2> | W | 0 | PLCDSP to A7 core IPC flag 2 clear.  Writing 1 to this bit clears the PLCTOA7IPCFLG<2> for the PLCDSP and PLCTOA7IPCSTS<2> for the A7.  Writing 0 has no effect. |
| 1 | PLCTOA7IPCCLR<1> | W | 0 | PLCDSP to A7 core IPC flag 1 clear.  Writing 1 to this bit clears the PLCTOA7IPCFLG<1> for the PLCDSP and PLCTOA7IPCSTS<1> for the A7.  Writing 0 has no effect. |
| 0 | PLCTOA7IPCCLR<0> | W | 0 | PLCDSP to A7 core IPC flag 0 clear.  Writing 1 to this bit clears the PLCTOA7IPCFLG<0> for the PLCDSP and PLCTOA7IPCSTS<0> for the A7.  Writing 0 has no effect. |

Notes: Normally, A7 will clear (acknowledge) the PLCTOA7 IPC event flags. This mechanism may be useful if RF DSP is non-responsive.

### PLCTOA7IPCFLG<15:0>

PLCDSP core to A7 core IPC flags register

Address Offset

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | PLCTOA7IPCFLG<15> | R | 0 | PLCDSP to A7 core IPC flag 15 status.  Indicates to PLCDSP whether thePLCTOA7IPCFLG<15> is set.  0: The event flag is not set  1: The event flag is set |
| 14 | PLCTOA7IPCFLG<14> | R | 0 | PLCDSP to A7 core IPC flag 14 status.  Indicates to PLCDSP whether thePLCTOA7IPCFLG<14> is set.  0: The event flag is not set  1: The event flag is set |
| 13 | PLCTOA7IPCFLG<13> | R | 0 | PLCDSP to A7 core IPC flag 13 status.  Indicates to PLCDSP whether thePLCTOA7IPCFLG<13> is set.  0: The event flag is not set  1: The event flag is set |
| 12 | PLCTOA7IPCFLG<12> | R | 0 | PLCDSP to A7 core IPC flag 12 status.  Indicates to PLCDSP whether thePLCTOA7IPCFLG<12> is set.  0: The event flag is not set  1: The event flag is set |
| 11 | PLCTOA7IPCFLG<11> | R | 0 | PLCDSP to A7 core IPC flag 11 status.  Indicates to PLCDSP whether thePLCTOA7IPCFLG<11> is set.  0: The event flag is not set  1: The event flag is set |
| 10 | PLCTOA7IPCFLG<10> | R | 0 | PLCDSP to A7 core IPC flag 10 status.  Indicates to PLCDSP whether thePLCTOA7IPCFLG<10> is set.  0: The event flag is not set  1: The event flag is set |
| 9 | PLCTOA7IPCFLG<9 | R | 0 | PLCDSP to A7 core IPC flag 9 status.  Indicates to PLCDSP whether thePLCTOA7 IPCFLG<9> is set.  0: The event flag is not set  1: The event flag is set |
| 8 | PLCTOA7IPCFLG<8> | R | 0 | PLCDSP to A7 core IPC flag 8 status.  Indicates to PLCDSP whether thePLCTOA7 IPCFLG<8> is set.  0: The event flag is not set  1: The event flag is set |
| 7 | PLCTOA7IPCFLG<7> | R | 0 | PLCDSP to A7 core IPC flag 7 status.  Indicates to PLCDSP whether thePLCTOA7 IPCFLG<7> is set.  0: The event flag is not set  1: The event flag is set |
| 6 | PLCTOA7IPCFLG<6> | R | 0 | PLCDSP to A7 core IPC flag 6 status.  Indicates to PLCDSP whether thePLCTOA7 IPCFLG<6> is set.  0: The event flag is not set  1: The event flag is set |
| 5 | PLCTOA7IPCFLG<5> | R | 0 | PLCDSP to A7 core IPC flag 5 status.  Indicates to PLCDSP whether thePLCTOA7 IPCFLG<5> is set.  0: The event flag is not set  1: The event flag is set |
| 4 | PLCTOA7IPCFLG<4> | R | 0 | PLCDSP to A7 core IPC flag 4 status.  Indicates to PLCDSP whether thePLCTOA7 IPCFLG<4> is set.  0: The event flag is not set  1: The event flag is set |
| 3 | PLCTOA7IPCFLG<3> | R | 0 | PLCDSP to A7 core IPC flag 3 status.  Indicates to PLCDSP whether thePLCTOA7 IPCFLG<3> is set.  0: The event flag is not set  1: The event flag is set |
| 2 | PLCTOA7IPCFLG<2> | R | 0 | PLCDSP to A7 core IPC flag 2 status.  Indicates to PLCDSP whether thePLCTOA7 IPCFLG<2> is set.  0: The event flag is not set  1: The event flag is set |
| 1 | PLCTOA7IPCFLG<1> | R | 0 | PLCDSP to A7 core IPC flag 1 status.  Indicates to PLCDSP whether thePLCTOA7 IPCFLG<1> is set.  0: The event flag is not set  1: The event flag is set |
| 0 | PLCTOA7IPCFLG<0> | R | 0 | PLCDSP to A7 core IPC flag 0 status.  Indicates to PLCDSP whether thePLCTOA7 IPCFLG<0> is set.  0: The event flag is not set  1: The event flag is set |

### A7TOPLCIPCACK<15:0>

A7 core to PLCDSP core IPC event acknowledge register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | A7TOPLCIPCACK<15> | W | 0 | A7 to PLCDSP core IPC event 15 acknowledge.  Writing 1 to this bit clears the A7TOPLCIPCFLG<15> and A7TOPLCIPCSTS<15> which are set by A7.  Writing 0 to this bit has no effect |
| 14 | A7TOPLCIPCACK<14> | W | 0 | A7 to PLCDSP core IPC event 14 acknowledge.  Writing 1 to this bit clears the A7TOPLCIPCFLG<14> and A7TOPLCIPCSTS<14> which are set by A7.  Writing 0 to this bit has no effect |
| 13 | A7TOPLCIPCACK<13> | W | 0 | A7 to PLCDSP core IPC event 13 acknowledge.  Writing 1 to this bit clears the A7TOPLCIPCFLG<13> and A7TOPLCIPCSTS<13> which are set by A7.  Writing 0 to this bit has no effect |
| 12 | A7TOPLCIPCACK<12> | W | 0 | A7 to PLCDSP core IPC event 12 acknowledge.  Writing 1 to this bit clears the A7TOPLCIPCFLG<12> and A7TOPLCIPCSTS<12> which are set by A7.  Writing 0 to this bit has no effect |
| 11 | A7TOPLCIPCACK<11> | W | 0 | A7 to PLCDSP core IPC event 11 acknowledge.  Writing 1 to this bit clears the A7TOPLCIPCFLG<11> and A7TOPLCIPCSTS<11> which are set by A7.  Writing 0 to this bit has no effect |
| 10 | A7TOPLCIPCACK<10> | W | 0 | A7 to PLCDSP core IPC event 10 acknowledge.  Writing 1 to this bit clears the A7TOPLCIPCFLG<10> and A7TOPLCIPCSTS<10> which are set by A7.  Writing 0 to this bit has no effect |
| 9 | A7TOPLCIPCACK<9 | W | 0 | A7 to PLCDSP core IPC event 9 acknowledge.  Writing 1 to this bit clears the A7TOPLCIPCFLG<9> and A7TOPLCIPCSTS<9> which are set by A7.  Writing 0 to this bit has no effect |
| 8 | A7TOPLCIPCACK<8> | W | 0 | A7 to PLCDSP core IPC event 8 acknowledge.  Writing 1 to this bit clears the A7TOPLCIPCFLG<8> and A7TOPLCIPCSTS<8> which are set by A7.  Writing 0 to this bit has no effect |
| 7 | A7TOPLCIPCACK<7> | W | 0 | A7 to PLCDSP core IPC event 7 acknowledge.  Writing 1 to this bit clears the A7TOPLCIPCFLG<7> and A7TOPLCIPCSTS<7> which are set by A7.  Writing 0 to this bit has no effect |
| 6 | A7TOPLCIPCACK<6> | W | 0 | A7 to PLCDSP core IPC event 6 acknowledge.  Writing 1 to this bit clears the A7TOPLCIPCFLG<6> and A7TOPLCIPCSTS<6> which are set by A7.  Writing 0 to this bit has no effect |
| 5 | A7TOPLCIPCACK<5> | W | 0 | A7 to PLCDSP core IPC event 5 acknowledge.  Writing 1 to this bit clears the A7TOPLCIPCFLG<5> and A7TOPLCIPCSTS<5> which are set by A7.  Writing 0 to this bit has no effect |
| 4 | A7TOPLCIPCACK<4> | W | 0 | A7 to PLCDSP core IPC event 4 acknowledge.  Writing 1 to this bit clears the A7TOPLCIPCFLG<4> and A7TOPLCIPCSTS<4> which are set by A7.  Writing 0 to this bit has no effect |
| 3 | A7TOPLCIPCACK<3> | W | 0 | A7 to PLCDSP core IPC event 3 acknowledge.  Writing 1 to this bit clears the A7TOPLCIPCFLG<3> and A7TOPLCIPCSTS<3> which are set by A7.  Writing 0 to this bit has no effect |
| 2 | A7TOPLCIPCACK<2> | W | 0 | A7 to PLCDSP core IPC event 2 acknowledge.  Writing 1 to this bit clears the A7TOPLCIPCFLG<2> and A7TOPLCIPCSTS<2> which are set by A7.  Writing 0 to this bit has no effect |
| 1 | A7TOPLCIPCACK<1> | W | 0 | A7 to PLCDSP core IPC event 1 acknowledge.  Writing 1 to this bit clears the A7TOPLCIPCFLG<1> and A7TOPLCIPCSTS<1> which are set by A7.  Writing 0 to this bit has no effect |
| 0 | A7TOPLCIPCACK<0> | W | 0 | A7 to PLCDSP core IPC event 0 acknowledge.  Writing 1 to this bit clears the A7TOPLCIPCFLG<0> and A7TOPLCIPCSTS<0> which are set by A7.  Writing 0 to this bit has no effect |

### A7TOPLCIPCSTS<15:0>

A7 core to PLCDSP core IPC event status register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | A7TOPLCIPCSTS<15> | R | 0 | A7 to PLCDSP core IPC event 15 status.  Indicates to PLCDSP whether the A7TOPLCIPC event 15 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 14 | A7TOPLCIPCSTS<14> | R | 0 | A7 to PLCDSP core IPC event 14 status.  Indicates to PLCDSP whether the A7TOPLCIPC event 14 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 13 | A7TOPLCIPCSTS<13> | R | 0 | A7 to PLCDSP core IPC event 13 status.  Indicates to PLCDSP whether the A7TOPLCIPC event 13 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 12 | A7TOPLCIPCSTS<12> | R | 0 | A7 to PLCDSP core IPC event 12 status.  Indicates to PLCDSP whether the A7TOPLCIPC event 12 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 11 | A7TOPLCIPCSTS<11> | R | 0 | A7 to PLCDSP core IPC event 11 status.  Indicates to PLCDSP whether the A7TOPLCIPC event 11 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 10 | A7TOPLCIPCSTS<10> | R | 0 | A7 to PLCDSP core IPC event 10 status.  Indicates to PLCDSP whether the A7TOPLCIPC event 10 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 9 | A7TOPLCIPCSTS<9 | R | 0 | A7 to PLCDSP core IPC event 9 status.  Indicates to PLCDSP whether the A7TOPLCIPC event 9 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 8 | A7TOPLCIPCSTS<8> | R | 0 | A7 to PLCDSP core IPC event 8 status.  Indicates to PLCDSP whether the A7TOPLCIPC event 8 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 7 | A7TOPLCIPCSTS<7> | R | 0 | A7 to PLCDSP core IPC event 7 status.  Indicates to PLCDSP whether the A7TOPLCIPC event 7 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 6 | A7TOPLCIPCSTS<6> | R | 0 | A7 to PLCDSP core IPC event 6 status.  Indicates to PLCDSP whether the A7TOPLCIPC event 6 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 5 | A7TOPLCIPCSTS<5> | R | 0 | A7 to PLCDSP core IPC event 5 status.  Indicates to PLCDSP whether the A7TOPLCIPC event 5 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 4 | A7TOPLCIPCSTS<4> | R | 0 | A7 to PLCDSP core IPC event 4 status.  Indicates to PLCDSP whether the A7TOPLCIPC event 4 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 3 | A7TOPLCIPCSTS<3> | R | 0 | A7 to PLCDSP core IPC event 3 status.  Indicates to PLCDSP whether the A7TOPLCIPC event 3 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 2 | A7TOPLCIPCSTS<2> | R | 0 | A7 to PLCDSP core IPC event 2 status.  Indicates to PLCDSP whether the A7TOPLCIPC event 2 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 1 | A7TOPLCIPCSTS<1> | R | 0 | A7 to PLCDSP core IPC event 1 status.  Indicates to PLCDSP whether the A7TOPLCIPC event 1 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |
| 0 | A7TOPLCIPCSTS<0> | R | 0 | A7 to PLCDSP core IPC event 0 status.  Indicates to PLCDSP whether the A7TOPLCIPC event 0 is set or not by A7.  0: No event is set by A7  1: An event is set by A7 |

Note: IPC event status 0-7 will trigger interrupt to the PLCDSP core via the GIC.

### PLCTORFIPCSET<15:0>

PLCDSP core to RFDSP core IPC set register

Address Offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | PLCTORFIPCSET<15> | W | 0 | PLCDSP to RFDSP core IPC flag 15 set.  Writing 1 to this bit sets the PLCTORFIPCFLG<15> for the PLCDSP and PLCTORFIPCSTS<15> for the RFDSP.  Writing 0 has no effect. |
| 14 | PLCTORFIPCSET<14> | W | 0 | PLCDSP to RFDSP core IPC flag 14 set.  Writing 1 to this bit sets the PLCTORFIPCFLG<14> for the PLCDSP and PLCTORFIPCSTS<14> for the RFDSP.  Writing 0 has no effect. |
| 13 | PLCTORFIPCSET<13> | W | 0 | PLCDSP to RFDSP core IPC flag 13 set.  Writing 1 to this bit sets the PLCTORFIPCFLG<13> for the PLCDSP and PLCTORFIPCSTS<13> for the RFDSP.  Writing 0 has no effect. |
| 12 | PLCTORFIPCSET<12> | W | 0 | PLCDSP to RFDSP core IPC flag 12 set.  Writing 1 to this bit sets the PLCTORFIPCFLG<12> for the PLCDSP and PLCTORFIPCSTS<12> for the RFDSP.  Writing 0 has no effect. |
| 11 | PLCTORFIPCSET<11> | W | 0 | PLCDSP to RFDSP core IPC flag 11 set.  Writing 1 to this bit sets the PLCTORFIPCFLG<11> for the PLCDSP and PLCTORFIPCSTS<11> for the RFDSP.  Writing 0 has no effect. |
| 10 | PLCTORFIPCSET<10> | W | 0 | PLCDSP to RFDSP core IPC flag 10 set.  Writing 1 to this bit sets the PLCTORFIPCFLG<10> for the PLCDSP and PLCTORFIPCSTS<10> for the RFDSP.  Writing 0 has no effect. |
| 9 | PLCTORFIPCSET<9 | W | 0 | PLCDSP to RFDSP core IPC flag 9 set.  Writing 1 to this bit sets the PLCTORFIPCFLG<9> for the PLCDSP and PLCTORFIPCSTS<9> for the RFDSP.  Writing 0 has no effect. |
| 8 | PLCTORFIPCSET<8> | W | 0 | PLCDSP to RFDSP core IPC flag 8 set.  Writing 1 to this bit sets the PLCTORFIPCFLG<8> for the PLCDSP and PLCTORFIPCSTS<8> for the RFDSP.  Writing 0 has no effect. |
| 7 | PLCTORFIPCSET<7> | W | 0 | PLCDSP to RFDSP core IPC flag 7 set.  Writing 1 to this bit sets the PLCTORFIPCFLG<7> for the PLCDSP and PLCTORFIPCSTS<7> for the RFDSP.  Writing 0 has no effect. |
| 6 | PLCTORFIPCSET<6> | W | 0 | PLCDSP to RFDSP core IPC flag 6 set.  Writing 1 to this bit sets the PLCTORFIPCFLG<6> for the PLCDSP and PLCTORFIPCSTS<6> for the RFDSP.  Writing 0 has no effect. |
| 5 | PLCTORFIPCSET<5> | W | 0 | PLCDSP to RFDSP core IPC flag 5 set.  Writing 1 to this bit sets the PLCTORFIPCFLG<5> for the PLCDSP and PLCTORFIPCSTS<5> for the RFDSP.  Writing 0 has no effect. |
| 4 | PLCTORFIPCSET<4> | W | 0 | PLCDSP to RFDSP core IPC flag 4 set.  Writing 1 to this bit sets the PLCTORFIPCFLG<4> for the PLCDSP and PLCTORFIPCSTS<4> for the RFDSP.  Writing 0 has no effect. |
| 3 | PLCTORFIPCSET<3> | W | 0 | PLCDSP to RFDSP core IPC flag 3 set.  Writing 1 to this bit sets the PLCTORFIPCFLG<3> for the PLCDSP and PLCTORFIPCSTS<3> for the RFDSP.  Writing 0 has no effect. |
| 2 | PLCTORFIPCSET<2> | W | 0 | PLCDSP to RFDSP core IPC flag 2 set.  Writing 1 to this bit sets the PLCTORFIPCFLG<2> for the PLCDSP and PLCTORFIPCSTS<2> for the RFDSP.  Writing 0 has no effect. |
| 1 | PLCTORFIPCSET<1> | W | 0 | PLCDSP to RFDSP core IPC flag 1 set.  Writing 1 to this bit sets the PLCTORFIPCFLG<1> for the PLCDSP and PLCTORFIPCSTS<1> for the RFDSP.  Writing 0 has no effect. |
| 0 | PLCTORFIPCSET<0> | W | 0 | PLCDSP to RFDSP core IPC flag 0 set.  Writing 1 to this bit sets the PLCTORFIPCFLG<0> for the PLCDSP and PLCTORFIPCSTS<0> for the RFDSP.  Writing 0 has no effect. |

### PLCTORFIPCCLR<15:0>

PLCDSP core to RFDSP core IPC event clear register

Address Offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | PLCTORFIPCCLR<15> | W | 0 | PLCDSP to RFDSP core IPC flag 15 clear.  Writing 1 to this bit clears the PLCTORFIPCFLG<15> for the PLCDSP and PLCTORFIPCSTS<15> for the RFDSP.  Writing 0 has no effect. |
| 14 | PLCTORFIPCCLR<14> | W | 0 | PLCDSP to RFDSP core IPC flag 14 clear.  Writing 1 to this bit clears the PLCTORFIPCFLG<14> for the PLCDSP and PLCTORFIPCSTS<14> for the RFDSP.  Writing 0 has no effect. |
| 13 | PLCTORFIPCCLR<13> | W | 0 | PLCDSP to RFDSP core IPC flag 13 clear.  Writing 1 to this bit clears the PLCTORFIPCFLG<13> for the PLCDSP and PLCTORFIPCSTS<13> for the RFDSP.  Writing 0 has no effect. |
| 12 | PLCTORFIPCCLR<12> | W | 0 | PLCDSP to RFDSP core IPC flag 12 clear.  Writing 1 to this bit clears the PLCTORFIPCFLG<12> for the PLCDSP and PLCTORFIPCSTS<12> for the RFDSP.  Writing 0 has no effect. |
| 11 | PLCTORFIPCCLR<11> | W | 0 | PLCDSP to RFDSP core IPC flag 11 clear.  Writing 1 to this bit clears the PLCTORFIPCFLG<11> for the PLCDSP and PLCTORFIPCSTS<11> for the RFDSP.  Writing 0 has no effect. |
| 10 | PLCTORFIPCCLR<10> | W | 0 | PLCDSP to RFDSP core IPC flag 10 clear.  Writing 1 to this bit clears the PLCTORFIPCFLG<10> for the PLCDSP and PLCTORFIPCSTS<10> for the RFDSP.  Writing 0 has no effect. |
| 9 | PLCTORFIPCCLR<9 | W | 0 | PLCDSP to RFDSP core IPC flag 9 clear.  Writing 1 to this bit clears the PLCTORFIPCFLG<9> for the PLCDSP and PLCTORFIPCSTS<9> for the RFDSP.  Writing 0 has no effect. |
| 8 | PLCTORFIPCCLR<8> | W | 0 | PLCDSP to RFDSP core IPC flag 8 clear.  Writing 1 to this bit clears the PLCTORFIPCFLG<8> for the PLCDSP and PLCTORFIPCSTS<8> for the RFDSP.  Writing 0 has no effect. |
| 7 | PLCTORFIPCCLR<7> | W | 0 | PLCDSP to RFDSP core IPC flag 7 clear.  Writing 1 to this bit clears the PLCTORFIPCFLG<7> for the PLCDSP and PLCTORFIPCSTS<7> for the RFDSP.  Writing 0 has no effect. |
| 6 | PLCTORFIPCCLR<6> | W | 0 | PLCDSP to RFDSP core IPC flag 6 clear.  Writing 1 to this bit clears the PLCTORFIPCFLG<6> for the PLCDSP and PLCTORFIPCSTS<6> for the RFDSP.  Writing 0 has no effect. |
| 5 | PLCTORFIPCCLR<5> | W | 0 | PLCDSP to RFDSP core IPC flag 5 clear.  Writing 1 to this bit clears the PLCTORFIPCFLG<5> for the PLCDSP and PLCTORFIPCSTS<5> for the RFDSP.  Writing 0 has no effect. |
| 4 | PLCTORFIPCCLR<4> | W | 0 | PLCDSP to RFDSP core IPC flag 4 clear.  Writing 1 to this bit clears the PLCTORFIPCFLG<4> for the PLCDSP and PLCTORFIPCSTS<4> for the RFDSP.  Writing 0 has no effect. |
| 3 | PLCTORFIPCCLR<3> | W | 0 | PLCDSP to RFDSP core IPC flag 3 clear.  Writing 1 to this bit clears the PLCTORFIPCFLG<3> for the PLCDSP and PLCTORFIPCSTS<3> for the RFDSP.  Writing 0 has no effect. |
| 2 | PLCTORFIPCCLR<2> | W | 0 | PLCDSP to RFDSP core IPC flag 2 clear.  Writing 1 to this bit clears the PLCTORFIPCFLG<2> for the PLCDSP and PLCTORFIPCSTS<2> for the RFDSP.  Writing 0 has no effect. |
| 1 | PLCTORFIPCCLR<1> | W | 0 | PLCDSP to RFDSP core IPC flag 1 clear.  Writing 1 to this bit clears the PLCTORFIPCFLG<1> for the PLCDSP and PLCTORFIPCSTS<1> for the RFDSP.  Writing 0 has no effect. |
| 0 | PLCTORFIPCCLR<0> | W | 0 | PLCDSP to RFDSP core IPC flag 0 clear.  Writing 1 to this bit clears the PLCTORFIPCFLG<0> for the PLCDSP and PLCTORFIPCSTS<0> for the RFDSP.  Writing 0 has no effect. |

Notes: Normally, RFDSP will clear (acknowledge) the PLCTORF IPC event flags. This mechanism may be useful if RF DSP is non-responsive.

### PLCTORFIPCFLG<15:0>

PLCDSP core to RFDSP core IPC flags register

Address Offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | PLCTORFIPCFLG<15> | R | 0 | PLCDSP to RFDSP core IPC flag 15 status.  Indicates to PLCDSP whether the PLCTORFIPCFLG<15> is set.  0: The event flag is not set  1: The event flag is set |
| 14 | PLCTORFIPCFLG<14> | R | 0 | PLCDSP to RFDSP core IPC flag 14 status.  Indicates to PLCDSP whether the PLCTORFIPCFLG<14> is set.  0: The event flag is not set  1: The event flag is set |
| 13 | PLCTORFIPCFLG<13> | R | 0 | PLCDSP to RFDSP core IPC flag 13 status.  Indicates to PLCDSP whether the PLCTORF IPCFLG<13>is set.  0: The event flag is not set  1: The event flag is set |
| 12 | PLCTORFIPCFLG<12> | R | 0 | PLCDSP to RFDSP core IPC flag 12 status.  Indicates to PLCDSP whether the PLCTORF IPCFLG<12> is set.  0: The event flag is not set  1: The event flag is set |
| 11 | PLCTORFIPCFLG<11> | R | 0 | PLCDSP to RFDSP core IPC flag 11 status.  Indicates to PLCDSP whether the PLCTORF IPCFLG<11> is set.  0: The event flag is not set  1: The event flag is set |
| 10 | PLCTORFIPCFLG<10> | R | 0 | PLCDSP to RFDSP core IPC flag 10 status.  Indicates to PLCDSP whether the PLCTORF IPCFLG<10>is set.  0: The event flag is not set  1: The event flag is set |
| 9 | PLCTORFIPCFLG<9 | R | 0 | PLCDSP to RFDSP core IPC flag 9 status.  Indicates to PLCDSP whether the PLCTORF IPCFLG<9> is set.  0: The event flag is not set  1: The event flag is set |
| 8 | PLCTORFIPCFLG<8> | R | 0 | PLCDSP to RFDSP core IPC flag 8 status.  Indicates to PLCDSP whether the PLCTORF IPCFLG<8> is set.  0: The event flag is not set  1: The event flag is set |
| 7 | PLCTORFIPCFLG<7> | R | 0 | PLCDSP to RFDSP core IPC flag 7 status.  Indicates to PLCDSP whether the PLCTORF IPCFLG<7> is set.  0: The event flag is not set  1: The event flag is set |
| 6 | PLCTORFIPCFLG<6> | R | 0 | PLCDSP to RFDSP core IPC flag 6 status.  Indicates to PLCDSP whether the PLCTORF IPCFLG<6> is set.  0: The event flag is not set  1: The event flag is set |
| 5 | PLCTORFIPCFLG<5> | R | 0 | PLCDSP to RFDSP core IPC flag 5 status.  Indicates to PLCDSP whether the PLCTORF IPCFLG<5> is set.  0: The event flag is not set  1: The event flag is set |
| 4 | PLCTORFIPCFLG<4> | R | 0 | PLCDSP to RFDSP core IPC flag 4 status.  Indicates to PLCDSP whether the PLCTORF IPCFLG<4> is set.  0: The event flag is not set  1: The event flag is set |
| 3 | PLCTORFIPCFLG<3> | R | 0 | PLCDSP to RFDSP core IPC flag 3 status.  Indicates to PLCDSP whether the PLCTORF IPCFLG<3> is set.  0: The event flag is not set  1: The event flag is set |
| 2 | PLCTORFIPCFLG<2> | R | 0 | PLCDSP to RFDSP core IPC flag 2 status.  Indicates to PLCDSP whether the PLCTORF IPCFLG<2> is set.  0: The event flag is not set  1: The event flag is set |
| 1 | PLCTORFIPCFLG<1> | R | 0 | PLCDSP to RFDSP core IPC flag 1 status.  Indicates to PLCDSP whether the PLCTORF IPCFLG<1> is set.  0: The event flag is not set  1: The event flag is set |
| 0 | PLCTORFIPCFLG<0> | R | 0 | PLCDSP to RFDSP core IPC flag 0 status.  Indicates to PLCDSP whether the PLCTORF IPCFLG<0> is set.  0: The event flag is not set  1: The event flag is set |

### RFTOPLCIPCACK<15:0>

RFDSP core to PLCDSP core IPC event acknowledge register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | RFTOPLCIPCACK<15> | W | 0 | RFDSP core to PLCDSP core IPC event 15 acknowledge.  Writing 1 to this bit clears the RFTOPLCIPCFLG<15> and RFTOPLCIPCSTS<15> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 14 | RFTOPLCIPCACK<14> | W | 0 | RFDSP core to PLCDSP core IPC event 14 acknowledge.  Writing 1 to this bit clears the RFTOPLCIPCFLG<14> and RFTOPLCIPCSTS<14> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 13 | RFTOPLCIPCACK<13> | W | 0 | RFDSP core to PLCDSP core IPC event 13 acknowledge.  Writing 1 to this bit clears the RFTOPLCIPCFLG<13> and RFTOPLCIPCSTS<13> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 12 | RFTOPLCIPCACK<12> | W | 0 | RFDSP core to PLCDSP core IPC event 12 acknowledge.  Writing 1 to this bit clears the RFTOPLCIPCFLG<12> and RFTOPLCIPCSTS<12> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 11 | RFTOPLCIPCACK<11> | W | 0 | RFDSP core to PLCDSP core IPC event 11 acknowledge.  Writing 1 to this bit clears the RFTOPLCIPCFLG<11> and RFTOPLCIPCSTS<11> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 10 | RFTOPLCIPCACK<10> | W | 0 | RFDSP core to PLCDSP core IPC event 10 acknowledge.  Writing 1 to this bit clears the RFTOPLCIPCFLG<10> and RFTOPLCIPCSTS<10> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 9 | RFTOPLCIPCACK<9 | W | 0 | RFDSP core to PLCDSP core IPC event 9 acknowledge.  Writing 1 to this bit clears the RFTOPLCIPCFLG<9> and RFTOPLCIPCSTS<9> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 8 | RFTOPLCIPCACK<8> | W | 0 | RFDSP core to PLCDSP core IPC event 8 acknowledge.  Writing 1 to this bit clears the RFTOPLCIPCFLG<8> and RFTOPLCIPCSTS<8> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 7 | RFTOPLCIPCACK<7> | W | 0 | RFDSP core to PLCDSP core IPC event 7 acknowledge.  Writing 1 to this bit clears the RFTOPLCIPCFLG<7> and RFTOPLCIPCSTS<7> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 6 | RFTOPLCIPCACK<6> | W | 0 | RFDSP core to PLCDSP core IPC event 6 acknowledge.  Writing 1 to this bit clears the RFTOPLCIPCFLG<6> and RFTOPLCIPCSTS<6> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 5 | RFTOPLCIPCACK<5> | W | 0 | RFDSP core to PLCDSP core IPC event 5 acknowledge.  Writing 1 to this bit clears the RFTOPLCIPCFLG<5> and RFTOPLCIPCSTS<5> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 4 | RFTOPLCIPCACK<4> | W | 0 | RFDSP core to PLCDSP core IPC event 4 acknowledge.  Writing 1 to this bit clears the RFTOPLCIPCFLG<4> and RFTOPLCIPCSTS<4> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 3 | RFTOPLCIPCACK<3> | W | 0 | RFDSP core to PLCDSP core IPC event 3 acknowledge.  Writing 1 to this bit clears the RFTOPLCIPCFLG<3> and RFTOPLCIPCSTS<3> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 2 | RFTOPLCIPCACK<2> | W | 0 | RFDSP core to PLCDSP core IPC event 2 acknowledge.  Writing 1 to this bit clears the RFTOPLCIPCFLG<2> and RFTOPLCIPCSTS<2> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 1 | RFTOPLCIPCACK<1> | W | 0 | RFDSP core to PLCDSP core IPC event 1 acknowledge.  Writing 1 to this bit clears the RFTOPLCIPCFLG<1> and RFTOPLCIPCSTS<1> which are set by PLCDSP.  Writing 0 to this bit has no effect |
| 0 | RFTOPLCIPCACK<0> | W | 0 | RFDSP core to PLCDSP core IPC event 0 acknowledge.  Writing 1 to this bit clears the RFTOPLCIPCFLG<0> and RFTOPLCIPCSTS<0> which are set by PLCDSP.  Writing 0 to this bit has no effect |

### RFTOPLCIPCSTS<15:0>

RFDSP core to PLCDSP core IPC event status register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:16 | reserved |  |  | Reserved |
| 15 | RFTOPLCIPCSTS<15> | R | 0 | RFDSP core to PLCDSP core IPC event 15 status.  Indicates to PLCDSP whether the RFTOPLCIPC event 15 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 14 | RFTOPLCIPCSTS<14> | R | 0 | RFDSP core to PLCDSP core IPC event 14 status.  Indicates to PLCDSP whether the RFTOPLCIPC event 14 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 13 | RFTOPLCIPCSTS<13> | R | 0 | RFDSP core to PLCDSP core IPC event 13 status.  Indicates to PLCDSP whether the RFTOPLCIPC event 13 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 12 | RFTOPLCIPCSTS<12> | R | 0 | RFDSP core to PLCDSP core IPC event 12 status.  Indicates to PLCDSP whether the RFTOPLCIPC event 12 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 11 | RFTOPLCIPCSTS<11> | R | 0 | RFDSP core to PLCDSP core IPC event 11 status.  Indicates to PLCDSP whether the RFTOPLCIPC event 11 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 10 | RFTOPLCIPCSTS<10> | R | 0 | RFDSP core to PLCDSP core IPC event 10 status.  Indicates to PLCDSP whether the RFTOPLCIPC event 10 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 9 | RFTOPLCIPCSTS<9 | R | 0 | RFDSP core to PLCDSP core IPC event 9 status.  Indicates to PLCDSP whether the RFTOPLCIPC event 9 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 8 | RFTOPLCIPCSTS<8> | R | 0 | RFDSP core to PLCDSP core IPC event 8 status.  Indicates to PLCDSP whether the RFTOPLCIPC event 8 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 7 | RFTOPLCIPCSTS<7> | R | 0 | RFDSP core to PLCDSP core IPC event 7 status.  Indicates to PLCDSP whether the RFTOPLCIPC event 7 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 6 | RFTOPLCIPCSTS<6> | R | 0 | RFDSP core to PLCDSP core IPC event 6 status.  Indicates to PLCDSP whether the RFTOPLCIPC event 6 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 5 | RFTOPLCIPCSTS<5> | R | 0 | RFDSP core to PLCDSP core IPC event 5 status.  Indicates to PLCDSP whether the RFTOPLCIPC event 5 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 4 | RFTOPLCIPCSTS<4> | R | 0 | RFDSP core to PLCDSP core IPC event 4 status.  Indicates to PLCDSP whether the RFTOPLCIPC event 4 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 3 | RFTOPLCIPCSTS<3> | R | 0 | RFDSP core to PLCDSP core IPC event 3 status.  Indicates to PLCDSP whether the RFTOPLCIPC event 3 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 2 | RFTOPLCIPCSTS<2> | R | 0 | RFDSP core to PLCDSP core IPC event 2 status.  Indicates to PLCDSP whether the RFTOPLCIPC event 2 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 1 | RFTOPLCIPCSTS<1> | R | 0 | RFDSP core to PLCDSP core IPC event 1 status.  Indicates to PLCDSP whether the RFTOPLCIPC event 1 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |
| 0 | RFTOPLCIPCSTS<0> | R | 0 | RFDSP core to PLCDSP core IPC event 0 status.  Indicates to PLCDSP whether the RFTOPLCIPC event 0 is set or not by PLCDSP.  0: No event is set by PLCDSP  1: An event is set by PLCDSP |

Note: IPC event status 0-7 will trigger interrupt to the PLCDSP core via the GIC.

### A7TOPLCIPCTEST<31:0>

A7 To PLC Interrupt test register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:8 | reserved |  |  | Reserved |
| 7:0 | A7TOPLCIPCTEST | R/W | 0 | To force IPC\_A7TOPLC\_INT to be triggered, it is for debugging purpose only.  When write 1 to any bit of A7TOPLCIPCTEST, corresponding bit on IPC\_A7TOPLC\_INT[7:0] is asserted  When write 0, A7TOPLCIPCTEST has no effect on IPC\_A7TOPLC\_INT[7:0] |

### RFTOPLCIPCTEST<31:0>

RF To PLC Interrupt test register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:8 | reserved |  |  | Reserved |
| 7:0 | RFTOPLCIPCTEST | R/W | 0 | To force IPC\_RFTOPLC\_INT to be triggered, it is for debugging purpose only.  When write 1 to any bit of RFTOPLCIPCTEST, corresponding bit on IPC\_RFTOPLC\_INT[7:0] is asserted  When write 0, RFTOPLCIPCTEST has no effect on IPC\_RFTOPLC\_INT[7:0] |

### RFTOPLCACK\_INT\_CLR<31:0>

RF to PLC ACK interrupt clear register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:1 | reserved |  |  | Reserved |
| 0 | RFTOPLCACK\_INT\_CLR | W | 0 | To clear RF to PLC ACK interrupt flag  When write 1, RFTOPLC\_ACK\_INT is cleared |

### A7TOPLCACK\_INT\_CLR<31:0>

A7 to PLC ACK interrupt clear register

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:1 | reserved |  |  | Reserved |
| 0 | A7TOPLCACK\_INT\_CLR | W | 0 | To clear A7 to PLC ACK interrupt flag  When write 1, A7TOPLC\_ACK\_INT is cleared |

### PLCSRP00REQ<31:0>

Shared RAM page0 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 0 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP01REQ<31:0>

Shared RAM page1 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 1 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP02REQ<31:0>

Shared RAM page2 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 2 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP03REQ<31:0>

Shared RAM page3 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 3 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP04REQ<31:0>

Shared RAM page4 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page4 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP05REQ<31:0>

Shared RAM page5 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 5 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP06REQ<31:0>

Shared RAM page6 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 6 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP07REQ<31:0>

Shared RAM page7 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page7 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP08REQ<31:0>

Shared RAM page8 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 8 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP09REQ<31:0>

Shared RAM page9 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 9 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP10REQ<31:0>

Shared RAM page10 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page1 0 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP11REQ<31:0>

Shared RAM page11 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 11 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP12REQ<31:0>

Shared RAM page12 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 12 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP13REQ<31:0>

Shared RAM page13 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 13 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP14REQ<31:0>

Shared RAM page14 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 14 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP15REQ<31:0>

Shared RAM page15 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page15 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP16REQ<31:0>

Shared RAM page16 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 16 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP17REQ<31:0>

Shared RAM page17 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page17 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP18REQ<31:0>

Shared RAM page18 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 18 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP19REQ<31:0>

Shared RAM page19 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 19 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP20REQ<31:0>

Shared RAM page20 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 20 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP21REQ<31:0>

Shared RAM page21 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 21 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP22REQ<31:0>

Shared RAM page22 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 22 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP23REQ<31:0>

Shared RAM page23 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 23 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP24REQ<31:0>

Shared RAM page24 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 24 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP25REQ<31:0>

Shared RAM page25 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 25 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP26REQ<31:0>

Shared RAM page26 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 26 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP27REQ<31:0>

Shared RAM page27 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 27 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP28REQ<31:0>

Shared RAM page28 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 28 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP29REQ<31:0>

Shared RAM page29 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 29 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP30REQ<31:0>

Shared RAM page30 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 30 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### PLCSRP31REQ<31:0>

Shared RAM page31 ownership request semaphore register.

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:4 | key | W | 0 | Writing the value 0x58AF6C1 will allow writes to the SEM bits or writes are ignored. Reads will return 0.  Note: This is to prevent spurious writes to the semaphore bits. |
| 3:2 | reserved |  |  | Reserved |
| 1:0 | Sema4 | W | 0 | Shared RAM page 31 write access request semaphore from PLCDSP:  Write a value “11” to request the ownership;  Write a value “00” to relinquish the ownership. |

### Share RAM registers

### SHRAM\_DATA<31:0>

32Kbyte Shared RAM is accessible at address (0ffset) space of 0x00~0x1FFF

Address offset:

| Bits | Name | R/W | Reset | Description |
| --- | --- | --- | --- | --- |
| 31:0 | Shram\_data | R/W | 0 | Share RAM read/write data  Support 8/16/32-bit AHB transfer |

# Interface

|  |  |  |  |
| --- | --- | --- | --- |
| Terminal name | I/O | Description | Connection |
| HCLK | I | AHB clock | CLOCK MANAGEMENT |
| HRESETN | I | AHB bus reset | RESET MANAGEMENT |
| HADDR\_A7[31:0] | I | AHB address | COMM AHB bus |
| HWDATA\_A7[31:0] | I | AHB write data | COMM AHB bus |
| HWRITE\_A7 | I | AHB write signal | COMM AHB bus |
| HTRANS\_A7[1:0] | I | AHB transfer type | COMM AHB bus |
| HSEL\_A7 | I | AHB select | COMM AHB bus |
| HADDR\_RF[31:0] | I | AHB address | COMM AHB bus |
| HWDATA\_RF [31:0] | I | AHB write data | COMM AHB bus |
| HWRITE\_RF | I | AHB write signal | COMM AHB bus |
| HTRANS\_RF[1:0] | I | AHB transfer type | COMM AHB bus |
| HSEL\_RF | I | AHB select | COMM AHB bus |
| HADDR\_PLC[31:0] | I | AHB address | COMM AHB bus |
| HWDATA\_PLC [31:0] | I | AHB Write data | COMM AHB bus |
| HWRITE\_PLC | I | AHB Write signal | COMM AHB bus |
| HTRANS\_PLC[1:0] | I | AHB transfer type | COMM AHB bus |
| HSEL\_PLC | I | AHB select | COMM AHB bus |
| HADDR\_SHRAM[31:0] | I | AHB address | COMM AHB bus |
| HWDATA\_ SHRAM [31:0] | I | AHB Write data | COMM AHB bus |
| HWRITE\_ SHRAM | I | AHB Write signal | COMM AHB bus |
| HTRANS\_ SHRAM [1:0] | I | AHB transfer type | COMM AHB bus |
| HSEL\_ SHRAM | I | AHB select | COMM AHB bus |
| HRDATA\_A7[31:0] | O | AHB Read data | COMM AHB bus |
| HRESP\_A7[1:0] | O | AHB transfer response | COMM AHB bus |
| HREADYOUT\_A7 | O | AHB transfer done | COMM AHB bus |
| HRDATA\_RF[31:0] | O | AHB Read data | COMM AHB bus |
| HRESP\_RF[1:0] | O | AHB transfer response | COMM AHB bus |
| HREADYOUT\_RF | O | AHB transfer done | COMM AHB bus |
| HRDATA\_PLC[31:0] | O | AHB Read data | COMM AHB bus |
| HRESP\_PLC[1:0] | O | AHB transfer response | COMM AHB bus |
| HREADYOUT\_PLC | O | AHB transfer done | COMM AHB bus |
| HRDATA\_SHRAM[31:0] | O | AHB Read data | COMM AHB bus |
| HRESP\_SHRAM[1:0] | O | AHB transfer response | COMM AHB bus |
| HREADYOUT\_SHRAM | O | AHB transfer done | COMM AHB bus |
|  |  |  |  |
| SCAN\_MODE | I | SCAN mode setting  High : SCAN mode  Low : Normal mode | TEST\_CTRL |
| IPC\_RFTOA7\_INT[7:0] | O | RFDSP’s interrupt request to A7 | ARM subsystem’s GIC |
| IPC\_PLCTOA7\_INT[7:0] | O | PLCDSP’s interrupt request to A7 | ARM subsystem’s GIC |
| IPC\_A7TORF\_INT | O | A7’s interrupt request to RFDSP | RF subsystem’s GIC |
| IPC\_PLCTORF\_INT | O | PLCDSP’s interrupt request to RFDSP | RF subsystem’s GIC |
| IPC\_A7TOPLC\_INT | O | A7’s interrupt request to PLCDSP | PLC subsystem’s GIC |
| IPC\_RFTOPLC\_INT | O | RFDSP’s interrupt request to PLCDSP | PLC subsystem’s GIC |
| PLCTOA7\_ACK\_INT[7:0] | O | Interrupt to A7 Core triggered by PLC DSP core’s ACK | ARM subsystem’s GIC |
| RFTOA7\_ACK\_INT[7:0] | O | Interrupt to A7 Core triggered by RF DSP core’s ACK | ARM subsystem’s GIC |
| A7TOPLC\_ACK\_INT | O | Interrupt to PLC DSP Core triggered by A7 Core’s ACK | PLC subsystem’s GIC |
| RFTOPLC\_ACK\_INT | O | Interrupt to PLC DSP Core triggered by RF DSP Core’s ACK | PLC subsystem’s GIC |
| A7TORF\_ACK\_INT | O | Interrupt to RF Core triggered by A7 Core’s ACK | RF subsystem’s GIC |
| PLCTORF\_ACK\_INT | O | Interrupt to RF Core triggered by PLC DSP core’s ACK | RF subsystem’s GIC |



Figure 4 Integration of IPC module